EECE 143
Lecture 0: Intro to Digital Laboratory

Syllabus * Class Notes

Laboratory Equipment

Experiment 0 * Experiment 1

Introduction

Instructor Information:

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Office Hours: M,W 3pm-4pm (or anytime I am available M-F 8-4pm)
Course Website: http://www.eng.mu.edu/~perezjc/eece143.html

Attendance Policy:
Attendance is mandatory for all lectures and labs.

More info...

Course Description:
Gaining experience in the design, assembly, testing, and trouble-shooting of digital electronic circuits. Experiments encompass a wide range of topics such as combinational circuits, sequential circuits, clock circuits, programmable logic devices, and microprocessors.

Prerequisites:
EECE 112 with a minimum grade of C; EECE 041 with a minimum grade of C; and either EECE 190, COEN 030, or BIEN 185 which may be taken concurrently. It is the responsibility of the student to ensure that these pre-requisites are met. Successful completion of EECE 143 with the proper sequence of prerequisites is a requirement for graduation.

Course Materials:

Required:
EECE 143 Digital Design Laboratory Manual and Class Notes (PrintWorld)
EECE 143 Component Kit
Engineering & Science Notebook (National 33-610)

ON Semiconductor, High-Speed CMOS Data Book
Motorola, M68HC11 Reference Manual, 1990.

Optional:
EECE Tool Kit
Digital Design Text for EECE 112

Each student is required to purchase a component package and notebook.
Each student is required to bring their own breadboard and tools to lab.

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More info...

Course Goals:
- Apply theory learned in EECE 112 including combinational and sequential circuit design, decoders, multiplexors, and programmable logic devices.
- Utilize CUPL software to program programmable logic devices.
- Write programs to use a microprocessor in control applications

Course Objectives:
By the end of this course, you should…
- Be able to design, build, test, troubleshoot, and evaluate digital circuits
- Be able to utilize computer software such as Electronic Work Bench, PSPICE, and CUPL.
- Be able to evaluate and revise designs as actual performance is reviewed.
- Be able to prepare a written report that effectively communicates the objective, the design procedure, the experimental results, and the conclusion for any project design.

TENTATIVE Laboratory Schedule

Laboratory	Title	Lecture Date	Laboratory Date
0	Introduction to Digital Lab	Jan 14	Jan 22,24
1	Boolean Implementation	Jan 14	Jan29,31
2	Standard Combinational Circuits	Feb 4	Feb 5,7
3	One shots, Clocks & Counters	Feb 4	Feb 12,14
4	Flip flops, Registers & Shift registers	Feb 11	Feb 19,21
5	Programmable Logic Devices 1	Feb 18	Feb 26,28
6	Programmable Logic Devices 2	Feb 25	Mar 5,7
7	Microprocessor 1 – Intro to Microcontrollers Written Report	Mar 4	Mar 19,21
8	Microprocessor 2 – Software	Mar 18,25	Apr 2,4
	Written Report Due	Mar 25	
9	Microprocessor 3 – Countdown timer	Apr 8,15	Apr 16,18,23,25
10	Microprocessor 10 – Soda Machine Controller	Apr 22	Apr 30, May 2
	Evaluation & SCOT	Apr 29	

Grading

One Introductory Lab @ 20 pts	20 points	93.0-100.0	A
Four Discrete Logic Labs @ 30 pts	120 points	89.0-92.9	AB
Two PLD Labs @ 30 pts	60 points	85.0-88.9	B
Four Microprocessor Labs @ 30 pts	120 points	81.0-84.9	BC
Eleven laboratory written reports @ 25 pts	275 points	77.0-80.9	C
Written Report	50 points	73.0-76.9	CD
Five Quizzes @ 10 pts	50 points	70.0-72.9	D
Lab Notebook	55 points	Below 70.0	F
Total	750 points		

Each Lab consists of a series of experiments or procedures. Each Lab (except the introductory lab) will be graded on the basis of 55 total points, with 10 points assigned to the preparation , 20 points assigned to the actual Lab work and 25 points assigned for laboratory written report.

Lab Teams: Lab teams consisting of two students will be formed during the first lab period. It is expected that both team members will contribute to **ALL** the lab work.

Laboratory Preparation: Each student is responsible for maintaining his/her own Laboratory Notebook. (National 33-610) The preliminary lab work of preparing data sheets, designing circuits, performing calculations, answering questions, etc. should be written in the Lab Notebook. Each student is required to perform pre-lab work and enter it into his/her notebook. The lab assistant will examine your notebooks during lab period and assign a grade based upon the quality and contents of your pre-lab work. At the end of the semester all notebooks will be collected for a final grade by the instructor.

Lab Work: Each lab team must be "checked out" by the TA. Check-out will be used to confirm that the actual lab work as recorded in the lab notebook has been completed and that the lab station has been properly cleaned up. The TA will initial and date all the data acquired during the lab period.

Each lab should be completed during the lab period. If a group is unable to complete the lab work, they may complete it in the Open Laboratory or in the digital laboratory, if granted special permission by the instructor. The work must be checked to verify that all laboratory exercises are complete. All lab work should be completed before the next laboratory period.

Laboratory Written Reports: Reports are due one week after the lab section that lab work is to be performed at the beginning of the next lab period. Each written report shall include the following: a discussion of the goals of the laboratory, a description of the design of the circuitry involved in the laboratory, complete schematic diagrams, completed data tables, an analysis of your laboratory results and conclusion. Written reports should be typed double-spaced and all drawings should be done with a computer or hand-drawn NEATLY.

Written Research Report A 5-10 page written research report is required by each student. Students will perform research on one aspect of digital electronics and how it is used in industry and in the world today. Students are encouraged to perform research online as well as traditional means. Papers should be typed double-spaced and complete with a list of sources.

Assistance in the Lab: Students should be prepared to learn to operate most laboratory equipment with little or no help. The TA is available in the lab to help the students master the basic operation of the equipment, to monitor their safety and security, to assist the instructor in ensuring that proper and sufficient equipment/devices/ICs are available to the students to carry out the lab work, to monitor the security of the equipment, and to identify inoperative equipment and take appropriate steps for necessary repairs.

Although the TA and the instructor are available, students must take primary responsibility for the design, construction, trouble-shooting, and operation of their circuits. The TA and/or the instructor are not responsible for debugging the circuits, verifying the designs and checking the circuit wiring.

Notebook Format

Cover: "EECE 143", EECE 143 Digital Electronics Laboratory, "Lab Notebook", your name(s), Semester and Year, Lab Section number.

1st page: Table of Contents -- Experiment #, Title, Date, Page #s
2nd page: blank
3rd page and more: **Experiments**
Pre-Lab
Title, Name(S), Date
Equipment Check List: Device, Mue #
General Pre-Lab Questions And Problems.
Schematic Diagram Or Circuit Diagram With Parts List
Data Tables And Results
Empty Columns For Measured Data
Completed Theoretical Data
Comments Section
Troubleshooting Summary

Sample Prelab

Combinational Boolean Implementations
Experiment #1

Bruce Hoeppner & Teresa Allen
8 JAN 93

Equipment: Brown Cross station

	Device	Manufacturer	Model	MUE#
√	Oscope	HP	1652B	231365
√	Design Station	E&L Instr.	CADET	21107
√	DMM	HP	3435A	9694

Part 1:
AND-OR Implementation $A = w'x + wx'$

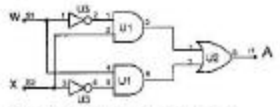


Figure 1-1A: Schematic for A = w'x + wx'

Function	Part#	IC#	Vcc	GND
AND	74HC08	U1	14	7
OR	74HC32	U2	14	7
NOT	74HC04	U3	14	7

Sample Prelab (2)

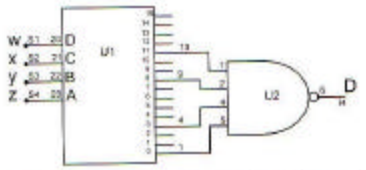
Part 1A Data

		Theoretical	Measured
w	x	A	A
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Part 1A Comments

(parts 1B, and C here!)

Part 1D Decoder*-NAND Implementation
D(w,x,y,z) = S (0,3,8,11)



Function	Part#	IC#	Vcc	GND
Decoder	74HC154	U1	24	12
NAND	74HC20	U2	14	7

Sample Prelab (3)

(remainder of Part D)

(rest of Experiment 1 Parts)

Troubleshooting Summary

1. Several ICs were not connected to power rail +5V. (Part1, 2)
2. Check for connections to IC enables. 74HC154's G1* and G2* were left off of pre-lab schematics. ICs don't work when not enabled.

Questions and Answers

1. What is the advantage of 2-level circuit implementations over 3 or more levels?

Answers go here ...

Laboratory #0: Digital lab Introduction

Purpose:

Learn to use the Agilent 54622D Mixed Signal Oscilloscope functions

Learn to use the CADET II electronic training station

Experiment with digital ICs, Schmitt gates, and clock circuits.

Preparation:

Prepare your notebooks as described in Chapter 1 of the Class Notes.

Read the entire section of this laboratory exercise in this Laboratory Manual. Also read and familiarize yourself with the tutorial sections for the logic analyzer and CADET board. The tutorials are found in Chapter 2 of the Class Notes.

Prepare the necessary data tables in your notebook for each Experiment Procedure.

You may wish to pre-build the Schmitt gate clock circuit in Figure 0.1.

Experiment Procedure

Agilent 54622D Mixed Signal Oscilloscope Evaluation

This procedure requires the use of the Evaluation Card and the Mixed Signal Oscilloscope.

CADET function generator frequency measurement.

This procedure will will demonstrate how to take measurements with the Agilent 54622D Mixed Signal Oscilloscope Answer all questions in the spaces provided in the Laboratory 0 Data sheet.

CADET bounceless push-buttons, logic switches, and LED indicators (LEDIs).

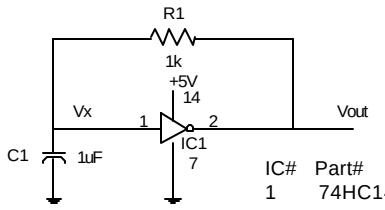
Connect two logic switches to two LEDIs. Connect each scope channel to one of the switches. Set scope for single-edge trigger on channel 1. Flip combinations of the switches. Measure the logic 0 and logic 1 voltages. Check for "bouncing." Connect a 560 Ω pull-up resistor from each bounceless push-button to +5 V. Connect the LEDIs and scope to the buttons. Repeat voltage measurements and check for "bouncing."

Experiment Procedure

Schmitt gate digital clock.

Assemble the circuit of Figure 0.1 Measure the output frequency, duty cycle, low voltage, high voltage and rise time using the HP1652B. Change C1 to three other values and repeat measurements. Change R1 to three other values and repeat measurements. Try to find the minimum and maximum frequencies.

Figure 0.1 Schmitt gate digital clock



IC#	Part#	Vcc	GND
1	74HC14	14	7

Logic Families

Transistor-Transistor Logic (TTL)

+ wide variety of functions and capabilities
+ good availability
+ low cost
+ easy to use
+ positive logic (theoretically simple)
+ high speed

- uses 5 Volt power supply
- consumes more power than other families
- typical active-low inputs and outputs

High-Speed CMOS (HC)

High Speed CMOS is not in the TTL family. However, it is designed to be functionally similar. Generally HC can be used in place of LS with a fanout restriction of 1.

+ very low power (HC µW vs TTL mW)
  - one CMOS transistor of the pair is always off
  - zero gate current
  - no internal resistors
+ variable supply voltage
  - 74HC 2.0 to 6.0 Volts (use three, or four, 1.5 V batteries)
  - 74C 3.0 to 15.0 Volts
  - CD4000 series 2.0 to 15.0 Volts
+ TTL replacements
+ high noise margin
+ can use pull-down or/and pull-up resistors

- handling
- speed

More Logic Families

CMOS 4000 Series

CMOS stands for Complementary Metal Oxide Semiconductor. Gates are made with pairs of MOS transistors (one N-channel, one P-channel). Typically, one of the two transistors is "off". This accounts for extremely low power consumption. Another advantages of 4000 series CMOS is a high noise margin. CMOS gates have high input impedance. Fanout is limited more by capacitive rather than by DC loading.

Emitter-Coupled Logic (ECL)

ECL gates have lower propagation delays (higher speeds) than TTL. Gates are designed so transistors do not saturate when they turn on. Logic 1 (High) is -0.8 V. Logic 0 (Low) is -1.8 V. Typically the circuit is powered with Vcc = GND, and Vee = -5.2V. A modern ECL NOR gate is Motorola's M10KH100. ECL noise immunity (0.25 V) is lower than TTL, or CMOS.

LOGIC FAMILY SPEED/POWER COMPARISON

Table 1

device	7400	74LS00	74ALS00	74HC00	74C00	CD4011	M10KH1
speed	10 ns	9.5 ns	5 ns	9 ns	50 ns	65 ns	1 ns
power	10 mW	2 mW	1 mW	25 µW	10 nW	10 nW	25 mW

speed = tpd (typical) power = Vcc * Icc (per gate)

Logic IC Naming

mm74xxxnnnrp

mm	Manufacturer
74 or 54	Temperature Range
xxx	Technology Type
nnn	Logic Function
r	Revision
pp	Package Type

Manufacturer -- mm

SN	Texas Instruments, Motorola
DM	National Semiconductor
none	Signetics

Pinouts will be the same for different manufacturers. Specifications may be slightly different.

Temperature Range -- 74 or 54

74	Standard (Commercial)	0 to 70 °C
54	Military	-55 to 125 °C

Pinouts may be different for the same function, and technology type, but different temperature range.

Technology Type -- xxx

TTL includes different types of integrated circuits with the same logic function. These differences are based on the type and size of transistors and diodes, and resistor values. These variations primarily affect the power and speed of the device. The following table summarizes speed and power using standard TTL as the base. High Speed CMOS is not in the TTL family. However, it is designed to be functionally similar. Generally HC can be used in place of LS with a fanout restriction of 1 LS device. Others: AC, ACT, BCT

Type	Speed	Power	Name
	std.	std.	Standard
H	high	high	High Power
L	low	low	Low Power
LS	std.	low	Low Power Schottky
S	high	high	Schottky
ALS	high	low	Advanced Low Power Schottky
AS	v. high	std.	Advanced Schottky
F	v. high	high	Fast TTL
HC	std.	v. low	High Speed CMOS
HCT	std.	v. low	High Speed CMOS with TTL Inputs
C	low	v. v. low	CMOS -- TTL Pinouts

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Logic Function -- nnn

Two to four digits identifies the logic function performed by the IC.

Table 1 Example TTL Parts

Part Number	Description
7400	Quad 2-Input NAND Gate
74LS00	Quad 2-Input NAND Gate
74LS01	Quad 2-Input NAND with Open-Collector Output
74LS32	Quad 2-Input OR Gate
74LS74A	Dual D-Type Positive-Edge-Triggered Flip-Flop with Preset and Clear
74LS138A	3:8 Decoder/Demultiplexer
74LS161A	4-Bit Synchronous Counter with Direct Clear
74LS636	8-Bit Parallel Error Detection and Correction Circuit with 3-State Output

Revision -- r
Improvements to an IC that correct slight errors or glitches have a letter suffix. The basic function of the circuit has not changed. The previous device becomes obsolete. Possible example: 74LS161 vs 74LS161A

Packaging -- pp

Table 1 Texas Instruments TTL Packaging

pp	Type	Package Name	Comments
J	DIP	Ceramic Dual-In-line Package	14 to 20 pins, 0.3" centers
JW	DIP	Ceramic Dual-In-line Package	24 pins, 0.6" centers
JT	DIP	Ceramic Dual-In-Line Package	24 pins, 0.3" centers
N	DIP	Plastic Dual-In-Line Package	14 to 40 pins, 0.3" or 0.6"
W	FP	Ceramic Dual Flat Package	14 to 24 pins, surf. mount
D	SOP	Small Outline Package	0.244" wide
DW	SOP	Wide Small Outline Package	0.410" wide, 16 or more pins
FK	LCC	Leadless Chip Carrier	square, surface mount only

Other TI packages: JD, JG, P

Experiment #1: Boolean Implementation

Goals:
1. Design circuits in specific combinational forms utilizing schematic diagrams.
2. Design circuits to minimize the number of ICs.
3. Gain experience in building and troubleshooting digital circuits.

Table E1.1 – Boolean Functions

A = wx+w'y	AND-OR
B = wx +w'y	NAND-NAND
C = (w+x)(x'+y')	NOR-NOR
D(w,x,y,z) = Σ(1,4,7,12)	Decoder-OR (Decoder*-NAND)
E(x,y,z) = Σ(3,4,5)	Multiplexer
F = x'y'z + xyz' + xyz	

Prelab:
1. Design a circuit for each of the given Boolean functions A, B, C, D, and E in the specific form. A schematic diagram is the final result of the design process. Use the minimum number of ICs for each function. Create a truth table for each function. Each truth table should include a column for: inputs, theoretical output and measured output. Complete the inputs and theoretical outputs section as part of Pre-Lab.

Table E1.2 – Boolean Functions

w	x	y	Theoretical A	Measured A

1. Design a circuit that implements functions D, E and F as one circuit with 3 outputs. Design to minimize the total number of ICs. Create a truth table for each function.

Design Rules:

Use 74HC (or 74LS) series ICs in your designs.

Experiment Procedure:

Build each of your circuit designs.
Keep circuits neat and organized. Use short wires.
Use top and bottom lines if breadboard for power and ground rails.

Test each of your circuit designs. A test plan is required for each circuit.

Things to remember

- Prelab, Prelab, Prelab. (Breadboarding circuits before lab can help)
- Come to all lab classes and lectures.
- Ask for help if you need it.
- Bring your components and databooks to lab.
- Bring your databooks and classnotes to each lecture in case of quiz.