Learning to Use IC's

Designing with Standard Combinational ICs: Adders, Comparators, Drivers & Buffers

Topics

- IC Specifications
- Switch Interfacing: SPST, DIP, BCD
- 7 Segment Displays & Drivers
- Adders
- Comparators
- Experiment #2

Breadboarding Tips

1. Use a separate node rail for power and ground. Use the top line for +5 V, and the bottom for ground.
2. Anytime an IC is inserted, **immediately** connect it to power and ground rails.
3. Insert ICs an logical order. Insert all ICs in with the same orientation. Good placement reduces wiring complexity.
4. Cut wires to smallest usable size. Keep your wires short.
5. Change wire colors often. Try to use Red for +5 V, and Black for ground.
6. Highlight or somehow record on the schematics as connections are made.
8. Label inputs and outputs using tape.
9. Connect discrete components directly to IC/nodes.
10. Do not twist resistor or capacitor leads to get exact values. Use a node on the breadboard. (Typically, digital circuits do not need exact values.)
11. Break each circuit into simple blocks. A block consists of a single IC or logic level. Assemble and test one block at a time.
12. Have one partner wire the circuit while the other records data. If something goes wrong, switch places. Sometimes it is easier to find someone else's mistake.
13. Alternate assembler and recorder positions after each experiment section so both partners get experience.
14. Split up very large circuits so that each partner assembles a section.
15. Keep power and clock lines short. Especially between boards.

DC Electrical Specifications

- Data sheets give "worst case" values.
- "Worst case" is the manufacturers guarantee of performance.
- The worst case can be a minimum or maximum depending on which would be less desirable.
- Typical values are sometimes given. These should be used for comparisons only. Worst case values should be used when designing circuits.

Voltages

A complete understanding of Boolean Algebra, and Digital Theory, can be achieved with the ideal inputs of **logic 1 = 5 V, and logic 0 = ground**. Real circuits provide a range of input and output voltages to allow for loss and noise.

High = most positive voltage in a binary system

Low = most negative voltage in a binary system

Positive Logic assigns a logic 1 to the most positive voltage.

Input Voltages

Vil low level input voltage

maximum voltage guaranteed to be accepted as a logic 0 at an input (min)

Vih high level input voltage

minimum voltage guaranteed to be accepted as a logic 1 at an input (max)

Output Voltages

Vol low level output voltage

maximum output voltage with input conditions applied that, according to the product specifications, will establish a logic 0 at the output. (max)

Voh high level output voltage

minimum output voltage with input conditions applied that, according to the product specifications, will establish a logic 1 at the output. (min)

Standard Combinational Circuits EECE143 Lecture 1

Logic Gate Currents

Ideal devices require zero current to operate, yet, can supply infinite current to a load. Real devices deviate from the ideal. TTL devices are made with NPN transistors ($I_c = \beta I_b$). TTL inputs will have some required input drive current. Also, a real device cannot supply infinite current. There are some limits. **IC currents are always specified as being into the device. Negative signs indicate current is leaving the device.**

Input Currents

Iil low-level input sink current

maximum current into an input when a low-level voltage is applied to that input.

Iih high-level input drive current

maximum current into an input when a high-level voltage is applied to that input.

Output Currents

Iol low-level output sink current

maximum (manufacturer guaranteed) current into an output when input conditions indicate the output should be low (logic 0).

Ioh high-level output source current

maximum current into an output when input conditions indicate the output should be high (logic 1).

Note: Although specified as a maximum, a specific devices may sink or source more current and still be within the correct voltage range. (i.e. Iout = 1 mA, for Vout = 3.0 V)

Propagation Delay

In idea logic devices, an input change, results in an immediate output change. In real devices, the output change is delayed. This delay is called propagation delay (tpd). Propagation delay is due to transistor switching, and circuit capacitance. tpd is a measure of the speed of a device. It is measured as two different values: propagation delay, high-to-low output, (tphl), and propagation delay, low-to-high output, (tplh). Measured with respect to the output irregardless of device function. Other propagation delay specifications related to switching from a logic value to or from a 3-state condition.

Maximum Clock Frequency fMAX

Flip-flops and other real clocked devices has a maximum clock frequency. fMAX is the highest clock speed at which the manufacturer guarantees the device will operate correctly. Note: Like many specs, an actual device may work at higher frequencies in a prototype, but, you should not exceed specs when designing for mass production.

Standard Combinational Circuits EECE143 Lecture 1

Power Requirements

Real ICs consume energy to operate. This energy is not used for external useful work. It is wasted (?) as heat. Typically, we would like this to be as small as possible.

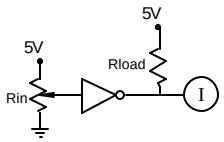
Power requirements vary the most between logic families.

IC power consumption is measured as **Icc * Vcc** with outputs open.

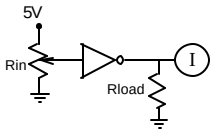
A 5 W power source can supply ≈100 74LS ICs at 50 mW each. Allowing for a margin of error, a limit of 20 is reasonable.

Note: Each LED in a circuit requires about the same amount of current as an IC. Decrease the number of ICs by one for each LED.

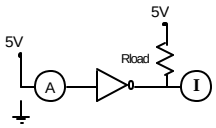
DC Spec Test Circuits



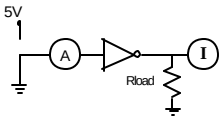
Vih Test Circuit



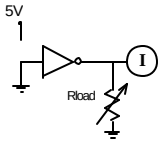
Vil Test Circuit



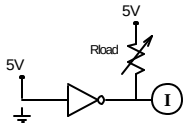
Iih Test Circuit



Iil Test Circuit



Voh, Ioh Test Circuit



Vol, Iol Test Circuit

Switch Interfacing: SPST

Interfacing an SPST to TTL Inputs

Use a pull-up resistor configuration.

0) **Logic 0**: Close Switch

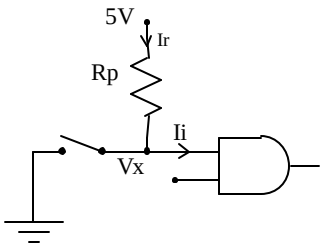
Vx is directly grounded.

∴ Logic 0

1) **Logic 1:** Open Switch

To be a logic 1 at the input Vx ≥ Vih.

∴ assume	Vx	≥	Vih	
	5.0 V - VR	≥	Vih	KVL: Vx = 5 V - VR
	5.0 V - Ir*Rp	≥	Vih	Ohm's Law: VR = Ir * Rp
	5.0 V - Iih*Rp	≥	Vih	Worst Case: Ir = Iih, (Ir ≤ Iih)
	5 V - 40 µA*Rp	≥	2.0 V	Iih = 40 µA, Vih = 2.0 V
	5.0 V	≥	2.0 V + 40 µA*Rp	
	5.0 V - 2.0V	≥	40 µA*Rp	
	3.0 V	≥	40 µA*Rp	
	3.0 V ÷ 40 µA	≥	Rp	
	75.000Ω	≥	Rp	
∴	Rp	≤	75 kΩ	



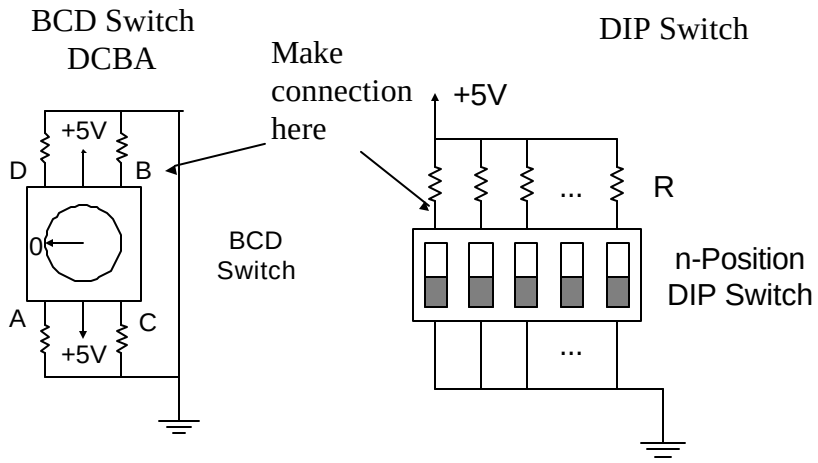
Rp ≤ 75 kΩ is the maximum value. Can Rp be 0Ω? ... 100 Ω.

↑ Rp ↓power wasted in Rp when the switch is closed.

↓ Rp ↑the noise margin for logic 1.

Example: Select Rp = 10 kΩ Vx = 5.0 V - (40 µA * 10 kΩ) = 4.6 V

More Switches

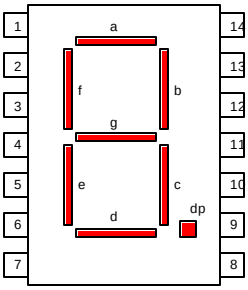


Decimal	4-bit binary w x y z		seven-segment a b c d e f g
0	0 0 0 0		1 1 1 1 1 1 0
1	0 0 0 1		0 1 1 0 0 0 0
2	0 0 1 0		1 1 0 1 1 0 1
3	0 0 1 1		1 1 1 1 0 0 1
4	0 1 0 0		0 1 1 0 0 1 1
5	0 1 0 1		1 0 1 1 0 1 1
6	0 1 1 0		1 0 1 1 1 1 1
7	0 1 1 1		1 1 1 0 0 0 0
8	1 0 0 0		1 1 1 1 1 1 1
9	1 0 0 1		1 1 1 0 0 1 1

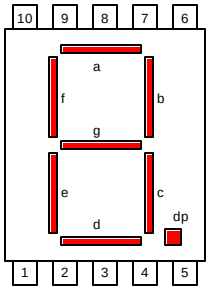
Seven Segment Displays

Seven-segment displays are used for decimal numeric displays. Seven light-emitting diodes are arranged so that all ten digits (0 - 9) can roughly be displayed.

Two Main IC Packages



14 pin DIP



10 pin wide DIP

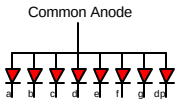
7-Segment Pinouts (typical)

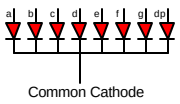
part#		FND507
segment	14-pin	10-pin
ca/cc	14	3,8
a	1	7
b	13	6
c	10	4
d	8	2
e	7	1
f	2	9
g	11	10
dp	9	5

7-Segment Display Information

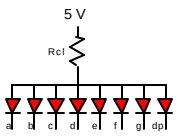
Common Cathode / Common Anode

To save pins on 7-seg packages, all LEDs typically share one pin for a common anode, or common cathode.

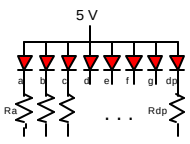




Current Limiting Resistors



Single
+ simple



Multiple
+ consistant brightness

Decimal Points

Seven-segment displays come with both right handed (RHDP), and left handed (LHDP) decimal points.

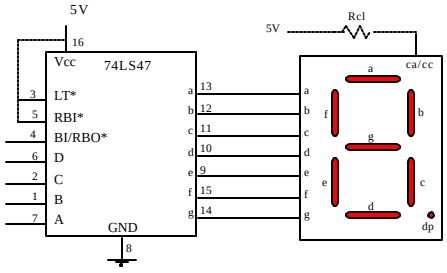
Multi-Segment Displays

Seven-segment displays are available in multiple segment packages. Two, or four digits are packaged together. Sometimes segment drive lines are multiplexed.

74LS47 BCD-to-7 Segment Decoder

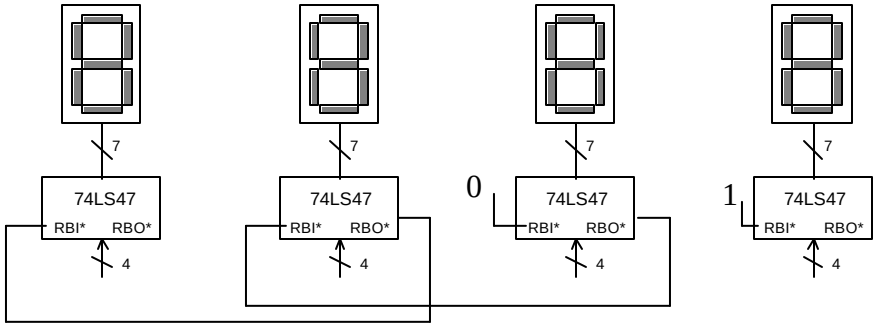
74LS47 BCD-to-7-Segment Decoder/Driver

Converts BCD data (digits 0 - 9, (4-bits)) into a 7-bit code used to drive 7-segment LED displays. Illegal BCD inputs are translated into indiscriminate, yet distinct display patterns. Data inputs to the code converter are: D, C, B, and A (lsb). Data outputs are: a, b, c, d, e, f, g; corresponding to the standard segment names of a 7-seg. display. Outputs are active-low, open-collector. The IC is designed to interface to common anode 7-segment displays. The 74LS47 has control inputs to test the segments, and blank leading zeros. Decimal points are not affected by the 74LS47.



Blanking Most Significant Digits

Multi-digit displays can be made where leading zeros are blanked. RBO* and RBI* control signals are daisy-chained to selectively blank digits. Any digit(s) that should always be displayed (with at least "0") should have the 74LS47 driver's RBI* set to 1. Any digit(s) that should be blanked when data is zero should have the driver's RBI* set to 0. Additional digits can be blanked when data is zero, and previous data is blanked (data is zero) by chaining the previous 74LS47 driver's RBO* to the present driver's RBI*.

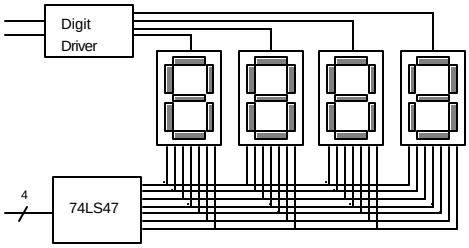


What if I want to use multiple displays and have only ONE 74LS47 driver?

MULTIPLEXED DISPLAYS

Multi-digit displays require a large number of signals (≈7 signals per digit). Multiplexing LED drive lines is one way of reducing the signal count. This method can reduce the number of drive signals to 7 + N. Where N is the number of digits.

The procedure sends 7 drive signals (a - g) to each of N digits' 7 cathodes (a - g). The common anodes of each N digits are driven one at a time while the correct data is presented to the cathodes. Precise timing is needed. The total number of signals is reduced.

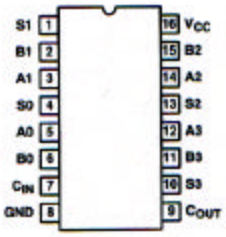


74HC283: 4-Bit Adder IC

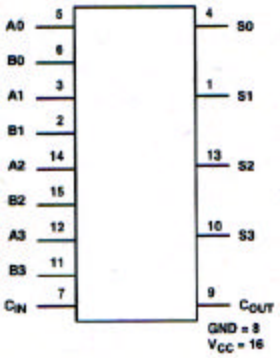
Use Carry Inputs and Outputs to create higher order Adders

Pinout

CD74HC283, CD74HCT283
(PDIP, SOIC)
TOP VIEW



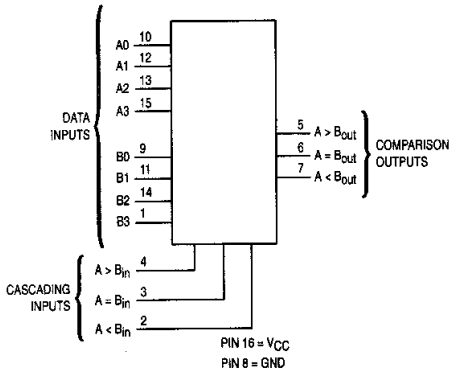
Functional Diagram



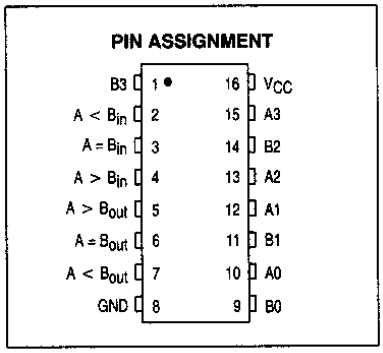
74HC85: 4-Bit Magnitude Comparator

- Use Cascading Inputs to create n-bit mag comparators
- See: www.ti.com >Semiconductor Products

LOGIC DIAGRAM



PIN ASSIGNMENT



Experiment #2: Standard Combinational Circuits

Goals:

Learn to use standard combinational & sequential ICs.

Build and use 7-segment display circuits.

Gain more experience understanding data book specifications: Vih, Vil...

Gain more experience testing digital circuit functions.

Learn about simple switch inputs with pull-up or pull-down resistors.

Prelab:

1. Design a decimal display circuit using 7-segment displays. Input numbers from a 4-position dipswitch or a BCD switch.
2. Design an 8-bit adder using 74HC ICs.
3. Design an 8-bit comparator using 74HC ICs.
4. Develop a test plan for each of your designs.
5. Complete the schematic diagrams to test High-speed CMOS input voltage specs. Compute values for load resistors.

Experiment Procedure:

Build and test each circuit.

Measure Vih, Vil.

Set CADET LED indicator switch to CMOS.

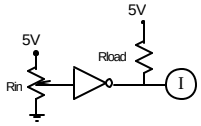
High-Level Input (Vih) Test

Assemble the HC high-level input voltage (Vih) test circuit for a 74HC04. Set Rload so that Iout equals data book Iol, when Vout equals data book Vol. Adjust Rin so Vin is 5.0 V. Is the output logic 0? (Is the green LED indicator (LEDI-G) on?) Measure Vout. Adjust Rin until LEDI-G goes off, then re-adjust so that it just turns on. Measure Vin. Vin is Vih Repeat for HCT and LS.

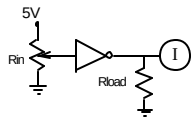
Low-level Input Voltage (Vil) Test

Assemble the HC low-level input voltage (Vil) test circuit. Set Rload so that Iout equals the databook Ioh, when Vout equals data book Voh. Set Rin so Vin is 0.0 V. Is the output logic 1? (Is the red LED indicator (LEDI-R) on?) Measure Vout. Adjust Rin until LEDI-R goes off then readjust so that it turns on. Measure Vin. Vin is Vil. Repeat for HCT and LS.

Log your Building, Testing, and Troubleshooting process.



Vih Test Circuit



Vil Test Circuit