

DESIGN NOTES FOR JFET Small Signal Amplifier Design

INTRODUCTION:

The design of (anything) is an iterative process. In order to meet stated specifications, you will need to answer many questions. As you make choices during the design, you must be prepared to discover that you have made improper choices, which will lead to redesign; however, you will learn from your "mistakes".

The purpose of your previous formal (classroom) instruction was to provide you with a "repertoire" of tools and methods you will be able to use to fulfill the design requirements. You have been introduced to the fundamentals of transistors and transistor amplifier topologies. The analysis process for transistor amplifiers follows a very set procedure, which may be summarized as

- (a) determine the DC operating point based on the circuit topology and the DC characteristics of the transistor, then
- (b) from the operating point information, determine the transistor's small signal model characteristics, and then
- (c) use that information to determine the AC operation of the amplifier circuit at midband, low frequency and high frequency.

When you analyze the circuit, you must realize that someone else designed it.

You have learned the **relative properties** of transistor amplifiers, such as which amplifier topology will have the "largest" voltage gain, which amplifier topology can have a "low" output resistance, which amplifier topologies have relatively high or low input resistances, which amplifier topologies can provide a large bandwidth, small bandwidth, etc. Knowledge of these properties gained through analysis must now be transferred into the design process. From analysis comes SYNTHESIS.

The most important thing to remember as you begin the design process is that you **MUST MAKE CHOICES**. When you design, each choice you make should be justifiable from the analysis you have done previously; each choice you make then "forces" other constraints or conditions which must be met, but the process does flow logically. Just don't forget, you **MUST MAKE CHOICES**.

The choices you will need to make in order to design a transistor amplifier to meet (or exceed) the stated specifications can be posed in the form of some "Design Questions" stated below:

- DQ-1) What type of circuit topology should be used for the AC small signal (ss) amplifier design?
- DQ-2) What type of transistor should be used?
BJT, FET, power?
- DQ-3) What type of circuit topology should be used for the DC bias design?
How is AC ss design affected by the DC bias design?
- DQ-4) What "model" transistor should be used?
2N2222A? 2N3904?....
- DQ-5) What are the unwritten specifications for the design?
temperature?
power?
any other constraints?
- DQ-6) Where does one START the design process?

The design process starts by unraveling the specifications and matching what you already know about transistor amplifiers with what is required for the design.

The Design Process:

In the rest of this material we're going to try to design an amplifier to meet or exceed the following specifications:

Design Statement: Design a transistor amplifier to provide a midband voltage gain of at least 10. The amplifier will be used to drive a 5000 Ω resistive load. The small signal (ss) source for the amplifier will have an output impedance of 600 Ω . The amplifier should have a bandwidth of at least 1 MHz, with a lower cutoff frequency no higher than 20 Hz.

Let's start by discussing the design statement

, The design specs indicate that the amplifier must provide VOLTAGE gain. This means that the amplifier might best be modeled with the VOLTAGE AMPLIFIER TOPOLOGY shown in figure 1. The amplifier we're designing is in the "dotted box". We still need to flesh in the details of what we will build, but this amplifier can be modeled as having an input impedance, R_{in} , an output impedance, R_{out} , and an open circuit voltage gain, $A_{v,oc}$. The source is modeled as an ideal source in series with the resistor R_s , and the load is modeled as the resistor R_{Load} .

, The design specs indicate that the amplifier should have an input impedance greater than 6 k Ω . Since we are using the voltage amplifier model, we want to make sure that v_{in} is as close to v_s as possible.

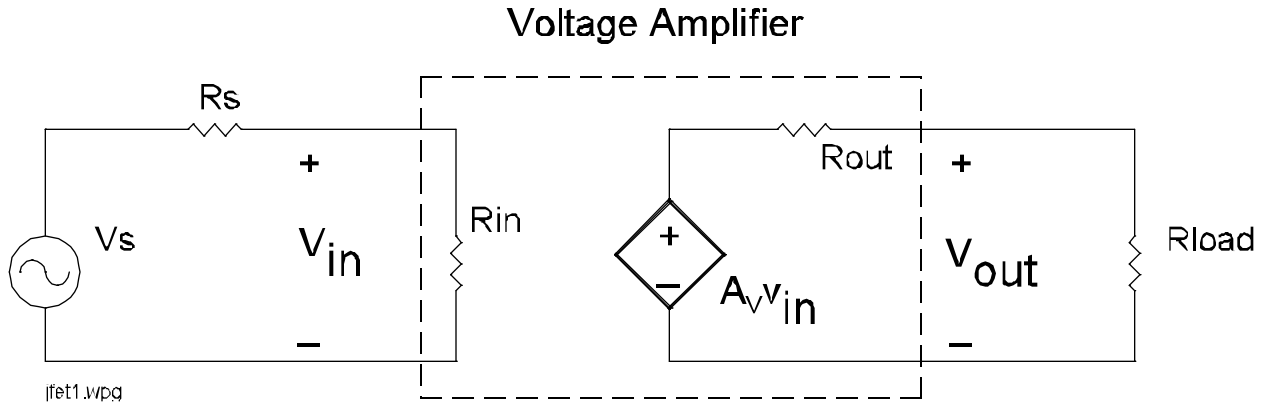


Figure 1: Voltage Amplifier Topology (jfet1_a.wpg)

Since $v_{in} = v_s R_{in}/(R_{in} + R_s)$, we can make v_{in} approximately equal to v_s by choosing R_{in} very much larger than R_s . A good rule of thumb ("ROT") is to use a factor of ten. Choosing a value of input impedance for the amplifier a factor of at least 10 greater than the output impedance of the source should "guarantee" that the amplifier will not LOAD the source. So we will choose to design our amplifier to have an input resistance of at least 6000 Ω . With that choice for R_{in} , $V_{in} \approx 0.9 V_s$.

The design specs indicate that the amplifier should have an output impedance on the order of 500 Ω or less. This is the "inverse" of the choice made above. This time the amplifier acts as the source to the load. To "guarantee" that the voltage supplied by the amplifier is directly transferred to the load (which is what we want), then there should be little, if any, voltage drop across the output resistance of the amplifier. To minimize this voltage drop, one should choose R_{out} a factor of at least 10 less than R_{load} if possible.

With these choices in mind, we've got a starting place to answer DQ-1. We want to use an amplifier topology that will provide a "healthy" voltage gain with a relatively high input impedance and a relatively low output impedance. These statements help to narrow the CHOICE of ac amplifier topology. And at this point, we should also try to implement this design with ONE stage if at all possible¹. It may be possible to use just one stage because a voltage gain of 10 is a relatively modest amount of gain.

By comparing the relative characteristics of BJT amplifier topologies, which include Common Emitter, (CE), Common Emitter with emitter resistor, (CE with R_E), Common Collector (emitter-follower) or Common Base and the FET amplifier topologies, Common Source (CS), Common Source with Source Resistor, (CS with R_{SS}), Common Drain or Common Gate...

A good choice for this design might be either a BJT CE or CE with R_E or the similar FET amplifier types, CS or CS with R_{SS} . These topologies have rather high output impedances however, and so we will...

¹KISS.

ASSUME that the load of $5\text{ k}\Omega$ is FIXED and will not vary. If we make this assumption (which may or may not be valid as one of the *unwritten specifications*), then we might be able to "design around" the low output impedance requirement. *This assumption will have a major impact on the rest of the design process. If we were designing this for a customer, we would first confirm this assumption with the customer before proceeding.*

We can now fill in some of the details for the amplifier. The area in the "dotted box" is starting to take shape as shown in figure 2. Note, however, that no choice has yet been made regarding the transistor type (denoted by a Q), OR the explicit form of the BIAS NETWORK. So far the only thing really done is to show that the output voltage will be tapped from the X-terminal which is either the collector terminal, if we choose a BJT, or the drain terminal, if we use an FET. And, of course, it's well known that these devices will need to be biased into the active region (for a BJT) or the saturation region (for an FET) if the device is to function as an amplifier. For now, V_{xy} and V_{yz} are placeholders for the real bias network we'll have to CHOOSE and then design.. The coupling capacitors, C_{in} and C_{out} , are also shown, because in general they would be in our amplifier circuit.

It's now time to answer the second design question, DQ-2.

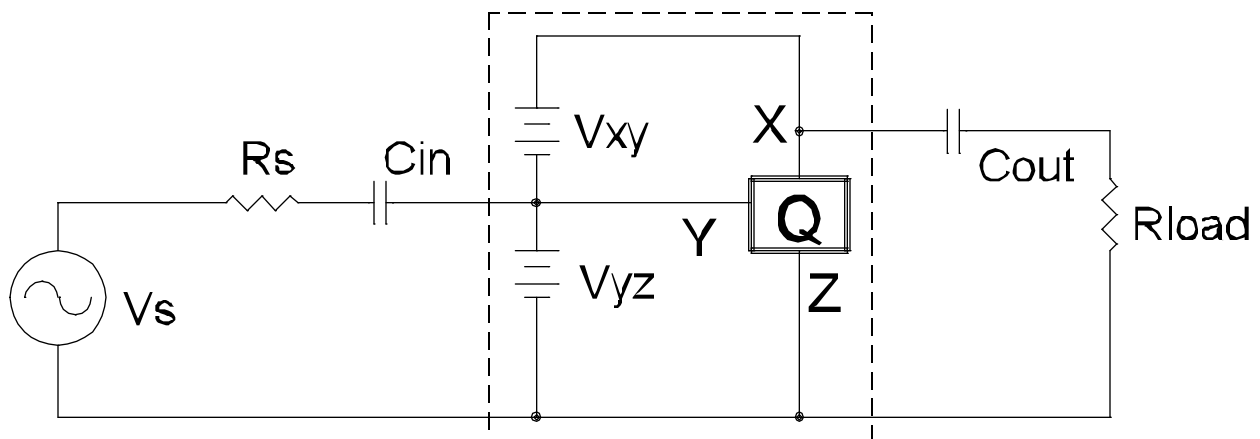


Figure 2: "Basic" Amplifier Topology for Design (jfet2_a.wpg)

What type of transistor should be used?

We're going to choose to use an n-channel JFET transistor; this means the "Q box" in figure 2 can be filled in with the appropriate symbol. This is not an arbitrary choice and some reasons for this choice are:

- a) In general, FET amplifiers will have greater bandwidth than equivalent BJT topologies. Since the input resistance for the FET is very large (modeled as infinite), the low frequency pole contributed by this resistance and C_{in} (pending a "reasonable" choice for C_{in}) will occur at low frequency. In addition, the device capacitances associated with FETs are generally smaller in value than those for a BJT. This has the effect of raising the upper cutoff frequency of an FET amplifier relative to an equivalent topology BJT amplifier.
- b) Even though (in general), an FET amplifier will have a smaller voltage gain than a BJT CE amplifier for roughly equivalent operating point currents, $I_{D,Q}$ and $I_{C,Q}$, the required voltage gain for the amplifier we're designing is fairly modest. So an FET should work as well as a BJT in this application, (BUT, we may be wrong).
- c) And now for the real reason. Since these notes are entitled "Design Notes for JFET Small Signal Amplifiers", why would we use a BJT?

Let's finish the rest of the picture by answering DQ-3,

What type of circuit topology should be used for the DC bias design?

Another VITAL component of your amplifier design is the CHOICE and DESIGN of the DC bias network. Something else that is important about the choice of the DC bias network for your amplifier design most often resides in the "unwritten" specifications for the design. Basically, you want the BEST DC bias circuit design. But how is "best" defined? One easy thing we can say about BEST at this stage is that, unless absolutely necessary, you do NOT want to use "two supply biasing" for the transistor. That's one more DC supply than you really need. However, there are some other issues to be considered as one chooses the "best" DC bias circuit topology.

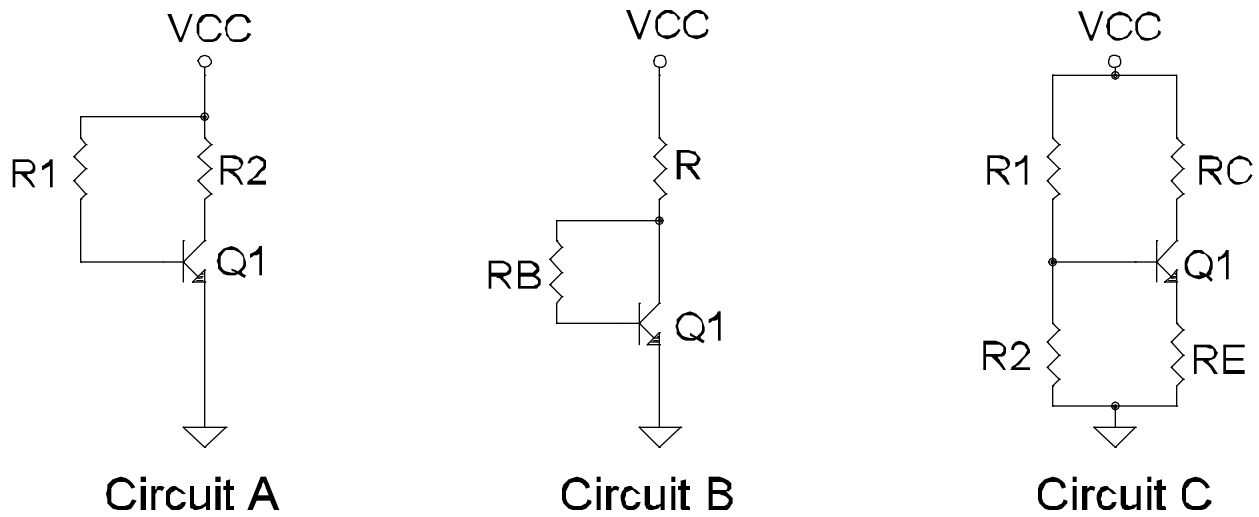
In general, the "best" bias circuit for a transistor amplifier is the bias circuit that will keep the Q-point parameters most stable with respect to changes in transistor characteristics and/or temperature. So with this definition of "best" in mind, you can **examine** several DC bias circuit topologies to determine which topology is indeed, best. There are many different bias networks that can be used. Several possible networks are shown in figure 3 (for both BJTs and FETs). Note that all of these circuits utilize "single supply" biasing techniques.

So which of these circuits is most stable? For FETs, the bias network on the RIGHT is the most stable of the two shown; this network is called the "voltage divider" bias network. For BJTs, the equivalent voltage divider bias network (circuit C) is also the most stable, but it turns out that circuit B (for BJTs) is almost as "good". When first seen, most students feel that this voltage divider biasing scheme is the most difficult to design. So, we'll choose that one to carry out the rest of the design work. (*I'm working under the assumption that if I show you the procedure for the "toughest", you'll be able to transfer the PROCESS of design to the "easier" ones.*)

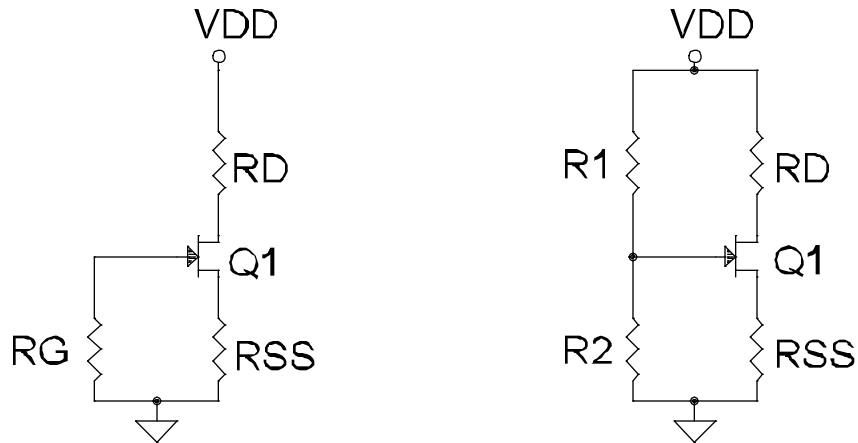
FINALLY, we've got the full circuit schematic for the amplifier we're going to design, it's shown in figure 4. Notice that a source resistor bypass capacitor, C_{ss} , has been added. This capacitor

Figure 3: Bias Circuit Topologies for BJT and FET transistors (jfet3_a.wpg)

BJT Bias Circuits



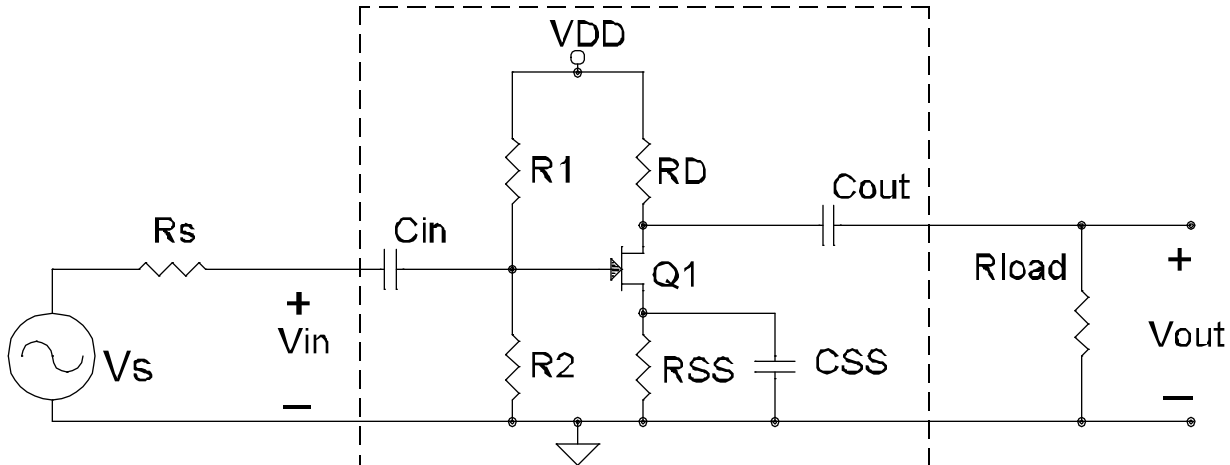
FET Bias Circuits



has been placed into the schematic because we truly want to design a Common Source (CS) amplifier in midband and not a common source with source resistor.

We've now got the schematic, but the work is NOT done because we've got to choose values for

Figure 4: Amplifier Topology for Design (jfet4_a.wpg)



the resistors, capacitors, dc supplies, and the "model number" of the JFET we're going to use. But without this circuit schematic, we wouldn't be able to do the rest of the "grunt work". This is the process we will embark upon now, but before we do so, here's some **PREPARATION ANALYSIS** (review) work you need to do.

Review problem (this problem is a paraphrase of problem 5.69 in the Sedra and Smith textbook):

When you do this problem, PLEASE do the analysis using the appropriate SYMBOLS. You WILL need the equations you generate as you continue reading through the rest of this introduction. Substitute the numerical values for the resistors, etc, only at the "very end". And as you do your review work, consider the following question:

How does the DC bias network affect ac small signal amplifier operation?

The JFET in the amplifier circuit of figure 4 has $V_p = -4\text{ V}$ and $I_{DSS} = 12\text{ mA}$; and at $I_D = 12\text{ mA}$, the output resistance of the FET, $r_o = 25\text{ k}\Omega$. The other component values are: $R_s = 100\text{ k}\Omega$, $R_1 = 1.4\text{ M}\Omega$, $R_2 = 0.6\text{ M}\Omega$, $R_D = 2.7\text{ k}\Omega$, $R_S = 2.7\text{ k}\Omega$, and $R_L = 2.7\text{ k}\Omega$.

- Determine the DC bias quantities I_D , V_{GS} , and V_D . (2.97 mA , -2.01 V , 12 V)
- Determine the value of g_m (transconductance gain for the FET) and r_o . (2.99 mA/V , $101\text{ k}\Omega$)
- Draw the small signal equivalent circuit for the amplifier using the small-signal model for the JFET.
- Determine the voltage gain, $A_{v_s} = v_o/v_s$, the input resistance of the amplifier, R_{in} and R_{out} , the output resistance of the amplifier. (-3.22 V/V , $0.42\text{ M}\Omega$, $2.6\text{ k}\Omega$)

As you did the work to get the answers for the problem above, you knew certain things which you then used to find the quantities requested. The same thing is true for design; some things you will KNOW, others you will need to FIND. For design, however, sometimes "find" means to

CHOOSE, at other times "find" means to CALCULATE.

Let's compare analysis and design. What is known and "to be found" for both analysis and design are shown in the table below.

	known	"to be found"
ANALYSIS	circuit topology transistor characteristics circuit component values	gain input and output resistances cutoff frequencies (low and high)
DESIGN	gain input and output resistances cutoff frequencies (low and high)	circuit topology transistor characteristics circuit component values

When you compare analysis and design, you should see that the things you know, and the things you must find simply trade places.

Obviously, **at this stage**, of our particular example design, we've moved the topology over into the known category, but there are still many more "unknowns" than "knowns".

From your analysis work you should be able to appreciate that the BIAS network and the TRANSISTOR parameters have a tremendous impact on the ac operation of the amplifier. The bias network is used to set $I_{D,Q}$, $V_{DS,Q}$ and $V_{GS,Q}$. The values for I_{DSS} and V_p for the transistor and $V_{GS,Q}$ and $I_{D,Q}$ determine the values for g_m and r_o for the transistor. These values, together with the value for R_D (which is part of the bias network), show up in the equation for the voltage gain and the output resistance for the amplifier. While it may look like a twisted mess, it's not. Here's the key...**CHOOSE THE TRANSISTOR. And so for our design we will choose to use the 2N3819 n-channel JFET**². This transistor has the following NOMINAL characteristics, $I_{DSS} = 12$ mA, $V_p = -3$ V, and $r_o = 20$ k Ω at $I_D = 12$ mA. Remember, this is a CHOICE, and it could be the wrong one, but even if the design DOESN'T work for the chosen transistor, we will have gained some insight into how to properly choose the transistor.

We've now answered all the design questions (we just answered DQ-4). Now we need to choose (calculate) values for R_1 , R_2 , R_D , R_S , and V_{DD} . Here are the "steps" we'll take.

²Why choose that particular JFET? The bottom line answer; because it's the one most likely to be in your component pack!!!

STEP 1: Find R_D

We're going to use the transistor characteristics, and the desired value for the midband voltage gain to "ballpark a figure" for the transconductance gain, g_m and the corresponding value for R_D . We'll then CHOOSE reasonable values for g_m and R_D , based not only on the desired A_v , but also the "target" R_{out} for the amplifier. Once we've got a value for g_m , we've also got a value for $V_{GS,Q}$, and, therefore, $I_{D,Q}$.

STEP 2: Find V_{DD} and R_{SS}

Using the value for $I_{D,Q}$ and R_D from step 1, we'll choose values for V_{DD} and R_{SS} to make sure that the JFET is biased in the saturation region.

STEP 3: Find R_1 and R_2

Using the values for $V_{GS,Q}$ and V_{DD} and the "target" R_{in} , we'll determine reasonable values for R_1 and R_2 .

STEP 4: Check the upper cutoff frequency for the amplifier

The upper cutoff frequencies are determined by the device capacitances, C_{gs} and C_{gd} , together with the resistors in the system which have now all been specified. We'll check to see if we've met the upper cut-off frequency requirement.

STEP 5: Choose C_{in} , C_{out} , and C_{SS}

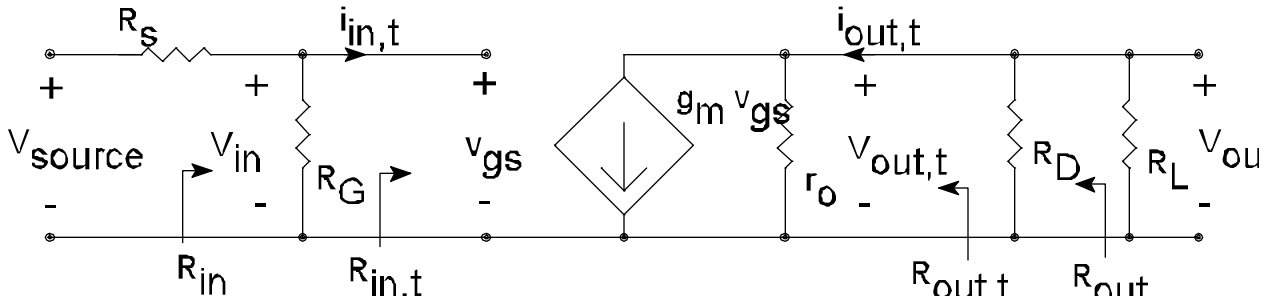
The input, output and bypass capacitors will be chosen to set the lower cutoff frequency at or below 20 Hz.

STEP 6: CHECK the design via simulation AND experimentation**DESIGN STATEMENT:**

Design a transistor amplifier to provide a midband voltage gain of at least 10. The amplifier will be used to drive a 5000 Ω resistive load. The small signal (ss) source for the amplifier will have an output impedance of at least 600 Ω . The amplifier should have a bandwidth of at least 1 MHz, with a lower cutoff frequency no higher than 20 Hz.

And so we begin the design process.....

Figure 5: AC small signal equivalent circuit of amplifier (jfet5_a.wpg)



STEP 1: Find R_D

Shown in figure 5 is the ac small signal equivalent circuit of the amplifier, including the ss model for the JFET³ (p.s., this is also the answer to part (c) of the review problem). The voltage gain for this amplifier, A_V is given by the following equation:

$$A_V = -g_m (r_o \parallel R_D \parallel R_{load}) . \tag{1}$$

What we want to do in this step is get some "ball park" estimates for g_m and R_D . We already know $R_{load} = 5 \text{ k}\Omega$, so *for design* we will ASSUME that r_o for the transistor is infinite. This assumption is not without some validity, because r_o is usually "largish". With this assumption, the equation for the midband voltage gain simplifies to,

$$A_V = -g_m (R_D \parallel R_{load}) , \tag{2}$$

and we can start making some estimates. Note that there is now a simple relation between g_m and R_D , so if we assume a value for R_D , we can readily calculate the corresponding value of g_m that will provide a voltage gain of 10. Remember, $R_{load} = 5 \text{ k}\Omega$. The results of this estimation of g_m based on R_D are shown in the table below.

In order to achieve a midband voltage gain of 10, then....

If $R_D =$ (value below), then	$R_D \geq R_{load} =$ (value below), and	g_m must equal (value below).
100 Ω	98 Ω	102 mA/V
1000 Ω	833 Ω	12 mA/V
10000 Ω	3.33 k Ω	3 mA/V

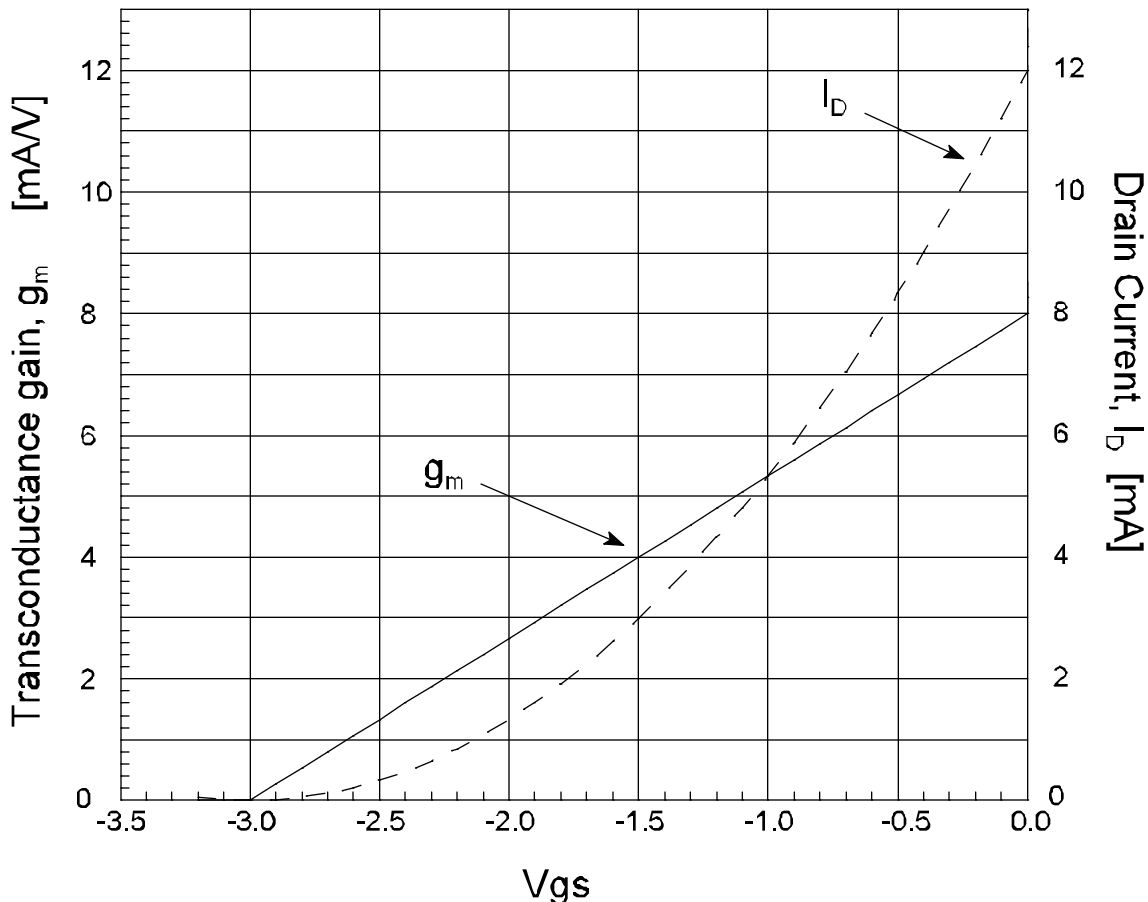
³Notice how the components for the JFET ss model are named. Remember, I told you in class that symbols change from one text book to another. Compare this model with the one you used in EECE 111. If the symbols are different, it does not mean that the concept is different.

What do these numbers mean, and how do they help us choose a value for g_m and R_D ? In order to answer those questions, we now have to consider the transistor and ask the question, what range of values for g_m can we reasonably expect to achieve with a 2N3819? The transconductance gain, g_m , for the transistor is a first order function of V_{GS} and depends on I_{DSS} and V_p as follows:

$$g_m(V_{GS}) = \frac{\partial I_D}{\partial V_{GS}} = 2 \frac{I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P} \right), \tag{3}$$

An n-channel JFET can be considered to be in the saturation region when V_{GS} is between V_p and 0. A plot of g_m as a function of V_{GS} in this range is shown in figure 6 with the transfer characteristic graph for the JFET superimposed on the figure (the transfer characteristic is the plot of I_D as a function of V_{GS}). What's important to note is that for a 2N3819 in the saturation region, g_m will only take on nominal values between 0 mA/V (when $V_{GS} = V_p$) and 8 mA/V (when $V_{GS} = 0$ V). Thus, using this knowledge and the preliminary calculations of table 2, we see that we can use the 2N3819, but only if we keep R_D "on the order" of 10 k Ω .

Figure 6: Transconductance of the 2N3819 (jfetgm.wpg)



We're now going to "tighten" this calculation for g_m and R_D , to specify design targets for these two quantities. **We will choose to design for a g_m value of 4 mA/V.** *This choice for g_m should result in the JFET being biased roughly in the middle of the saturation region.*

We can now determine a specific value for R_D . Using equation 2, with $*A_v* = 10$ V/V, $g_m = 4$ mA/V, and $R_L = 5$ k Ω , **we find that $R_D = 5$ k Ω .**

Let's consider the "target" output resistance value we've set for the amplifier. Under the assumption that r_o is infinite, the output resistance for the amplifier is EXACTLY equal to R_D . Now you see why the assumption was made that the load resistance would remain fixed in value at 5 k Ω . If we really needed a low output resistance from the amplifier we would need a low value for R_D . However, a low value for R_D means that we would NOT be able to bias the transistor into the saturation region⁴.

We're now going to check out the ramifications of the assumption we made that r_o is infinite, particularly to determine if the preliminary choices for g_m and R_D specified above together with the "real" value of r_o will still allow us to achieve the desired voltage gain. In order to do this check using equation 1, r_o must be determined. Besides being usually "largish" in value, r_o is also a function of I_D ,

$$r_o = \frac{V_A}{I_{D,Q}}, \quad (4)$$

where V_A is the Early Voltage. Using the nominal specification for the 2N3819 which has $r_o = 20$ k Ω when $I_D = 12$ mA, we can estimate that $V_A = 240$ V. From the graph of the transconductance gain as a function of V_{GS} , we find that g_m will be equal to 4 mA/V when $V_{GS,Q} = -1.5$ V. This value of $V_{GS,Q}$, in turn, determines $I_{D,Q}$; from the transfer characteristic plot (I_D versus V_{GS}), we see that 3 mA $< I_{D,Q} < 4$ mA, for $V_{GS,Q}$ provided that 5 V $< V_{DS,Q} < 25$ V. Using this range for $I_{D,Q}$, we can now calculate r_o ; for our choices, 60 k Ω $< r_o < 80$ k Ω .

Checking the gain using $g_m = 4$ mA/V, $R_D = 5$ k Ω , $R_{load} = 5$ k Ω and the two limits for r_o in equation 1, we find that $|A_v|$ will be between 9.6 V/V and 9.7 V/V, or at most 4% lower than what we're aiming for. Pretty good!!⁵

We now have one component value chosen, $R_D = 5$ k Ω . **We also know the operating point parameters for the transistor, $I_{D,Q} = (3$ to $4)$ mA, and $V_{GS,Q} = -1.5$ V.** We can now use these values to proceed to step 2.

⁴ If your customer told you that the load was NOT fixed, you have several options available to "fix" the design so you can achieve a low output resistance for the amplifier. One thing you could do is choose a different transistor. Another option would be to totally redesign the amplifier (YUCK, but maybe necessary). A third option might be to follow this stage with another amplifier stage. This second stage wouldn't need to provide any voltage gain, but ideally it would have an input resistance on the order of 5 kohm, and a low output resistance, such as a Common Drain (for an FET) or a Common Collector (for a BJT). And as a fourth option, FEEDBACK.

⁵ Now, we could go back and adjust g_m and R_D . And because we've laid out the process, we can now go back and think about it to "fine tune" our amplifier. However, we will NOT do this YET. (Remember the 10% rule?)

STEP 2: Find V_{DD} and R_{SS}

To determine values for V_{DD} and R_{SS} , we start with the "output loop" KVL equation from the bias network

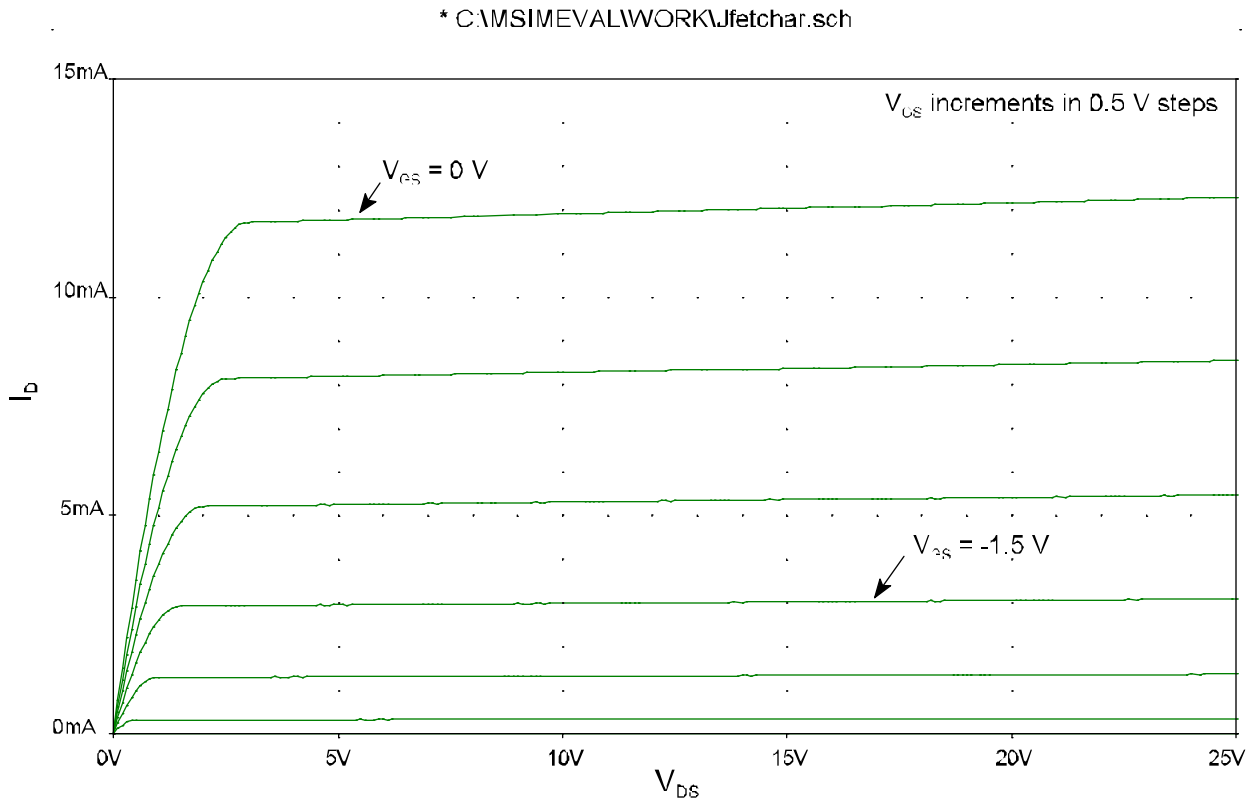
$$V_{DD} = \Delta V_{R_D} + V_{DS,Q} + \Delta V_{R_{SS}} \tag{5}$$

In this equation, only the voltage drop across R_D , is (currently) known, $\Delta V_{R_D} = I_{D,Q} R_D$. If

$V_{DS,Q}$ and the voltage drop across the resistor, R_{SS} , are chosen to ensure that the transistor is biased in the saturation region, then V_{DD} can be calculated. In order to proceed, we must **CHOOSE** reasonable values for $V_{DS,Q}$ and for R_{SS} .

To help choose $V_{DS,Q}$, the output characteristic curves (I_D as a function of V_{DS} for various values of V_{GS}) for the 2N3819 can give us some insight. This plot for the 2N3819 is shown in figure 7; the curve which corresponds to $V_{GS,Q} = -1.5$ V has been labeled on the graph. We need to choose $V_{DS,Q}$ to be some reasonable value along this curve; not "too close" to the ohmic region at low values of V_{DS} , and not "too high", where the curve is starting to curve up. So, **a good choice might be $V_{DS,Q} = 10$ V.**

Figure 7: Common Source Output Characteristics of J2N3819



Date: February 12, 1997

Now we will choose a value for the voltage drop across R_{SS} . Why is R_{SS} even in the circuit? You

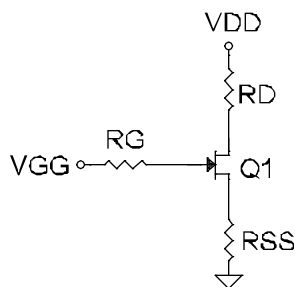
should remember that R_{SS} provides negative feedback for the bias network; this negative feedback is useful in stabilizing the Q-point parameters against changes in the transistor characteristics and temperature. A reasonable value for this voltage drop is on the order of 0.1 to 1 times the value of $V_{DS,Q}$, AND the value chosen must be larger than $|V_{GS,Q}|$. So for our case, let's choose this voltage drop to be equal to 4.5 V⁶. Since the current through this resistor is $I_{D,Q}$, the resulting calculated value for R_{SS} is 1.5 k Ω (assuming that $I_{D,Q} = 3$ mA). We use this calculated value for R_{SS} to choose the nearest standard value resistor (5% tolerance). **We can choose $R_{SS} = 1.5$ k Ω** (this is one of the few times that what is calculated turns out to be what is readily available). When you choose values for resistors, you have to make the decision to "round up" or "round down". Many times when I round (some resistor value) up, I will choose to round the "next" one down.

Because we've chosen the remaining voltage drops, it's a simple matter to calculate the value of V_{DD} :

$$\begin{aligned} V_{DD} &= \Delta V_{R_D} + V_{DS,Q} + \Delta V_{R_{SS}} \\ &= I_{D,Q}R_D + 10V + I_{D,Q}R_{SS} \\ &= 15V + 10V + 4.5V \\ &= 29.5V \approx 30V . \end{aligned}$$

So we will use $V_{DD} = 30$ V.

STEP 3: Find R_1 and R_2



These two resistors, together with V_{DD} , form the input bias network. The input side KVL equation can be written as

$$V_G = I_G R_G + V_{GS,Q} + I_{D,Q} R_{SS} \tag{6}$$

where the input bias network has been "thevenized"; as

$$V_G = V_{DD} \frac{R_2}{R_1 + R_2}, \text{ and } R_G = \frac{R_1 R_2}{R_1 + R_2} . \tag{7}$$

Since for an FET, $I_G = 0$, we can immediately calculate a value for $V_G = 3.0$ V using equation 6,

⁶Ok, this is not an obvious choice. Turns out that in the original version of this handout there was a math error further down the line. Also turns out that if I choose this voltage drop to be equal to 4.5 V, then only ONE other value would need to be changed. So I chose the "easy way" to fix my math error. In a sense, that's the beauty of design. And as an added benefit, this "new" design (to fix my math error) actually was better than the original.

since both $V_{GS,Q}$ and the voltage drop across R_{SS} are known⁷ ($V_G = -1.5 \text{ V} + 3 \text{ mA} \times 1.5 \text{ k}\Omega$). Using this value of V_G in equation 7 allows us to determine the relation between R_1 and R_2 ; for our values of $V_{DD} = 30 \text{ V}$ and $V_G = 3 \text{ V}$, we find that the value for R_1 should be equal to 9 times the value for R_2 . Thus, if we choose a value for R_2 , we can immediately calculate a value for R_1 .

Since we want the input resistance of the amplifier to be greater than $6 \text{ k}\Omega$, and the input resistance is the parallel combination of R_1 and R_2 , we've got a lot of latitude for our choice for R_2 . If we choose $R_2 = 100 \text{ k}\Omega$, then $R_1 = 900 \text{ k}\Omega$, and the input resistance that results from the parallel combination of those two resistors is $90 \text{ k}\Omega$ (a value definitely greater than $6 \text{ k}\Omega$).

In summary, at the completion of steps 1 through 3, we have specified all the resistors in the network and the value of the supply voltage:

$$R_{DD} = 5 \text{ k}\Omega; R_{SS} = 1.5 \text{ k}\Omega; R_1 = 900 \text{ k}\Omega; R_2 = 100 \text{ k}\Omega; \text{ and } V_{DD} = 30 \text{ V}.$$

STEP 4: Check the upper cutoff frequency for the amplifier

I'll let you do the arithmetic, but here's my answer for this check. Using the Miller approximation to "handle" the capacitor, C_{gd} , I find the two high frequency poles occur at 6.1 MHz and 16 MHz. Thus, the upper cutoff frequency for this amplifier is approximately 4.4 MHz, and we've exceeded our design goal.

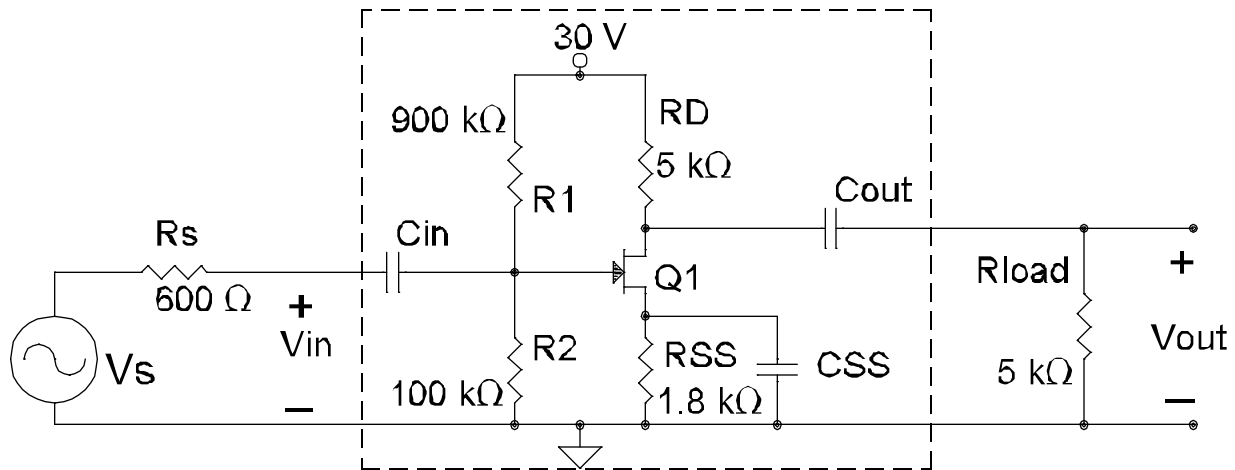
STEP 5: Choose C_{in} , C_{out} , and C_{SS}

Again, I'm going to let YOU do the arithmetic. I would choose the capacitor values so that the low frequency poles due to C_{in} , C_{out} and C_{SS} , can be calculated via a dominant pole technique with C_{SS} contributing the LOWEST frequency pole (so that it is well away from the dominant low frequency pole). A "convenient" arrangement of these poles might be assigned so that the poles contributed by C_{in} and C_{out} and C_{SS} could be ordered as 18.0 Hz, 1.0 Hz, and 1.0 Hz, respectively.

After you've calculated the values for these capacitors to achieve these frequencies, you must choose real capacitor values for the circuit you build. If you choose the nearest capacitor values GREATER than those you calculated, you will reduce the real value of the lower pole frequencies and hence, reduce the overall lower cutoff frequency for the amplifier.

⁷ The equation used to calculate $V_{GS,Q}$ from the known voltage drops also shows that the voltage drop across R_{SS} must be chosen to be greater in magnitude than $V_{GS,Q}$ or the resulting V_{GG} will have a NEGATIVE value. A negative valued V_{GG} would be impossible to physically achieve with the voltage divider bias network INPUT side.

Figure 7: The fully designed Amplifier



STEP 6: CHECK the design via simulation AND experimentation

The final circuit I came up with is shown above. When I SIMULATED the behavior of this circuit using PSPICE, I found the following:

Quantity	Design	From PSPICE	% difference
A_v	-9.6/-9.7 (19.65 dB, -180°)	- 9.74 (19.77 dB, -180°)	-1.5% (above)
upper cutoff frequency	4.4 MHz	24.9 MHz	-466 % (above)
lower cutoff frequency	20 Hz	16.5 Hz	17.5% (below)
$V_{GS,Q}$	-1.5 V	-1.5 V	
$I_{D,Q}$	3 mA - 4 mA	3.0 mA	
$V_{DS,Q}$	10 V	10.5 V	
g_m	4 mA/V	4.0 mA/V	
r_o	60-80 kS	NA	

In this table, percent difference is calculated as

$$\{ \text{"design value"} - \text{"PSPICE value"} \} / \{ \text{"design value"} \} \times 100.$$

ON PAPER, this design looks good.

The midband gain is within 10% of that specified by the customer, the lower cutoff frequency is less than 20 Hz, and the upper cutoff frequency dramatically exceeds the customer's

specifications. The midband gain and lower cutoff frequencies from the design (as simulated) look good. However, I'm curious (as should you be) as to why the results from PSPICE and the design check I did in step 4 are so wildly different. *What are possible reasons for this discrepancy?*

The above introduction to "how to design an amplifier" will serve as your starting point as you begin the work to design, build, and test a transistor amplifier to meet or exceed specifications which follow. I hope you have followed the process and understand it. The PROCESS for designing a BJT CE amplifier follows the same steps, taking into account the modifications to the process necessitated by the differences between the BJT and FET DC and AC characteristics. Appendix A to this guide points out the modifications to the process.

Virtually ALL the analysis work you have done previously in, for example, EECE 010 and EECE 111 has been used to implement the design process. If nothing else, this design example should have served to help you review all of that material. But that's the deal with design, previous analysis DOES lead to the ability to develop SYNTHESIS skills.

NOW FOR THE BAD NEWS.....

When the amplifier designed above was built and tested in the laboratory, the measured midband voltage gain was only 6.3 V/V, well below the "10% Rule" tolerance. How can something that looks so good on paper fail so miserable in practice?

I will point a finger at the SINGLE choice that was made that was solely responsible for this failure in the lab; **I CHOSE TO DESIGN WITH THE NOMINAL SPECIFICATIONS FOR THE TRANSISTOR.**

What does that word "nominal" mean? To attempt to answer that, here's definition 3 from my shelf copy of Webster's New Collegiate Dictionary,

¹nom-i-nal \ adj

3 a: existing or being something in name or form only < (as in) head of his party> 3 b: of, being, or relating to a designated or theoretical size that may vary from actual:

APPROXIMATE"

Nominal characteristics for a device are the characteristics that the device was (theoretically) designed to have. In the real world, however, manufacturing variability will inevitably lead to devices coming off the line and into the hands of the consumer which do not have these characteristics. So the manufacturer may also provide MIN/TYP/MAX values for the specifications.

Techniques exist to assist one in designing an amplifier which is tolerant of these device characteristic variabilities. If you're interested in pursuing this topic, I direct you to reference 2 in the bibliography at the end; there is an excellent design example for an FET amplifier which does take into account the MIN/MAX spread for some of the transistor's characteristics.

Alternatively, if one designs the amplifier based on the ACTUAL characteristics of the transistor

that will be used in the circuit, what looks good on paper should also look good in the lab. In other words, **if I had measured transfer characteristic and output characteristics for the 2N3819 for use in the appropriate steps in the design process above, the gain I measured would have been much closer to the gain for which I was designing.**

Appendix A - not available yet.

REFERENCES

The material in this design notes writeup has been drawn from many sources, including, but not limited to the following:

1. Webster's New Collegiate Dictionary, G. & C. Merriam Co, Springfield, MA, (1976), p 779.
2. William H. Hayt, Jr., and Gerold W. Neudeck, Electronic Circuit Analysis and Design, 2nd ed., Houghton Mifflin Company, Boston MA (1984).
3. Thomas C. Hayes and Paul Horowitz, The Student Manual for The Art of Electronics, Cambridge University Press, New York NY (1989).
4. Robert T. Paynter, Introductory Electronic Devices and Circuits, 2nd ed., Prentice Hall, chapter 9, pages 355-416.
5. Mark N. Horenstein, Microelectronic Circuits and Devices, Prentice Hall, Englewood Cliffs NJ (1990).
6. Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, 3rd ed., Holt Rinehart Winston, Philadelphia PA (1991).
7. Anne Eisenberg, Effective Technical Communication, McGraw Hill, New York NY (1982).