**COEN-4710: Computer Hardware**

**Credits/contact hours:** 3

**Course Coordinator:** Cristinel Ababei, Ph.D., Assistant Professor

**Text Book:** David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann, 2013, ISBN-10: 0124077269.

**Course Information:**

Overview of computer system design. Cost and performance specification. Design of arithmetic and logic units. Fundamentals of central processor architecture and a comparative study of computer instruction set architectures. Detailed study of microprocessors, including instruction execution timing and other timing considerations. Discussions of memory and I/O devices, including the interfaces to the CPU and I/O transfer techniques. Study of common bus standards.

**Prerequisites:** EECE-2030 and either EECE-2710 or COSC-2200.

**Required** course in the Computer Engineering program.

**Selected Elective** in ELEN Computer Hardware & Software area.

**Contribution to Professional Component:** Engineering Science 33 % / Engineering Design 67 %

**Course Goals:**

To present students with a detailed understanding of the design problems and their solutions for modern computer hardware at and above the circuit block diagram level.

**Course Objectives:**

*By the end of this course, you should....*

1. Compare hardware designs using quantitative performance measures, and identify the associated advantages and disadvantages of the designs.
2. Implement small to moderate-sized software applications using a modern assembly language (such as MIPS)
3. Design combinatorial and sequential hardware to perform basic arithmetic calculations, and be able to critique various design alternatives.
4. Design and implement a single-cycle datapath and its control signals, and be able to assess design methodologies and alternatives.
5. Design a basic pipelined datapath and its control signals at the circuit block diagram level, and to address issues with structural, data, or branching hazards at either the hardware or software level.
6. Design multiplication and division algorithms for integer or floating point numbers, using IEEE standard representation.
7. Design memory caches, interface memories at different levels of a memory hierarchy, and do a performance analysis of a hierarchical memory system.
8. Understand and intelligently discuss shared memory multiprocessors, clusters, hardware and software multithreading, and multiprocessor benchmarking.
9. Understand and intelligently discuss the field of computer architecture, and work effectively as a member of a design team in this field.

**Contribution to Student Outcomes**: partial fulfillment of Criterion 3 objectives A, C, E, G, H, I, J, K

**Course Topics:**

**Topic Textbook**

Introduction Chapter 1

Performance Analysis Chapter 1

Instruction sets, MIPS Chapter 2

Appendix A

Arithmetic Logic Units Chapter 3 (3.1-3.3)

Appendix B

Processor Datapath and Control Chapter 4

Appendix D

Pipelining Chapter 4

Multiplication, Division, Floating Point Chapter 3 (3.4-3.11)

Memory Hierarchy Chapter 5

Multicores, multiprocessors, clusters Chapter 6

Appendix C