**COEN-4730: Computer Architecture**

**Credits and contact hours:** 3.

 **Course coordinator:** Cristinel Ababei, Ph.D., Assistant Professor

**Text:** John L. Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufman, 2011, ISBN-10: 012383872X.

**Catalog description:** Review of basic computer architecture. Evaluation of architecture performance. Design and evaluation of instruction sets. Pipeline processors and instruction scheduling. Vector processors. Memory hierarchy and design including cache, main and virtual memories. Memory protection schemes. Input/output and its relation to system performance.

**Prerequisites:** Senior standing, 3.0 GPA, and COEN-4710 Computer Hardware; or consent of instructor.

**Selected Elective** in ELEN Computer Hardware & Software area, COEN Hardware area (breadth & depth)

**Professional component:**Engineering science 50 %
Engineering design 50 %

**Course Goals:**To provide students the ideas and concepts required to understand the architectures of modern microprocessors, including instruction set principles, instruction-level parallelism, memory hierarchy designs, and I/O; to provide students the analytical tools for assessing processor performance; and to provide students the opportunity to become familiar with the Internet and the technical literature as sources of current information on the topics of the course.

**Specific outcomes of instruction***By the end of this course, students should be able to perform the following tasks:*

1. Describe and utilize analytical tools for measuring and reporting processor performance.
2. Describe instruction set architectures and branch prediction.
3. Utilize techniques based on instruction- data- and thread- level parallelism to improve processor performance.
4. Describe memory/cache hierarchy.
5. Utilize optimization techniques to reduce cache misses, cache miss penalty, and cache hit time and to improve memory bandwidth.
6. Describe servers and warehouse scale computing.
7. Conduct simulation experiments using processor simulators to confirm the analysis done in class.
8. Prepare informative and organized reports that describe the methodologies employed, the results obtained, and the conclusions made in a simulation experiment. Prepare review-type reports of selected technical research articles.

**Student outcomes addressed by the course:**Partial fulfillment of Criterion 3 objectives A, C, E, I, J

**Brief list of topics to be covered**

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| **Week** | **Topics** | **Reading** |
| 1 | Introduction | Ch 1  |
| 2 | Review #1: Processors | Appendix A, C  |
| 3 | Review #2: Memory Architecture | Appendix B  |
| 4 | Advanced Cache Optimizations | Ch 2  |
| 5 | Contemporary Main Memory Design | Ch 2  |
| 6,7 | Advanced Instruction Level Parallelism (ILP) | Ch 3  |
| 8,9,10 | Beyond ILP: Thread Level Parallelism (TLP)Data Level Parallelism (DLP): SIMD, Vector Machines, GPUs | Ch 3Ch 4 |
| 11,12,13 | Coherence MechanismsServers | Ch 5  |
| 14,15 | Warehouse Scale Computing | Ch 6  |
| 16 | Final projects  |  |