**EECE 2030: Digital Electronics**

**Fall 2010**

**Course Description:**

Introduction to the basic principles of digital circuit analysis and design. Topics covered include: Boolean Algebra, number systems, basic logic gates, standard combinational circuits, combinational design, timing diagrams, flip-flops, standard sequential circuits, sequential design, and programmable logic devices.

**This is a required** class for the Electrical Engineering and Computer Engineering programs and for the Bioelectronics and Biocomputing majors in the Biomedical Engineering program.

**Prerequisites:** Junior Standing

**Course Goals:** To enable students to understand the circuit behavior of electronic switching devices and to acquire the tools of analysis and design of combinational and sequential logic circuits.

**Course Objectives:**

*By the end of this course, you should....*

1. Know the basic postulates and theorems of Boolean algebra and be able to use them to prove logic theorems and/or simplify logic expressions.
2. Be able to minimize logic expressions using Boolean algebra, Karnaugh Maps, and Computer Algorithms.
3. Know the symbols and functions of various combinational and sequential logic devices and be able to use these devices in logic design. The devices include (but are not limited to):

 AND, OR, NOT, XOR, XNOR, NAND, and NOR gates,

 Flip-Flops (RS, JK, T, and D),

 MSI and LSI logic devices such as MUXs, Encoders/Decoders, ROM, Counters,

 Registers and PLDs.

1. Be able to design digital circuits using combinational and sequential logic devices to implement a specified function.
2. Be able to use timing diagrams as an analysis tool, a design tool and a troubleshooting tool.
3. Be able to visualize a logic design problem from an initial problem statement in order to develop a state diagram for the solution.
4. Be able to translate a state diagram into a logic circuit design.

**Digital Electronics Topics:**   **In the Roth Tex**

 **Introduction/Review:** (5%)

 Number Systems Chapter 1

 Coding Schemes Chapter 1

 **Combinational Logic & Circuits:** (40%)

 Boolean Algebra Chapters 2 and 3

 Digital Gates (discrete)

AND/OR/Not Chapters 2

XOR, Equivalence Chapter 3

Minimization Techniques

Minterm/Maxterm expansion Chapter 4

Karnaugh maps Chapter 5

Quine-McCluskey Method Chapter 6

Multi-level circuits, NAND & NOR Chapter 7

MUXs, Decoders, Programmable Devices, ROM Chapter 9

Combination Circuit Design Chapter 8

 **Sequential Circuits:** (45%)

 Flip-Flops and Latches Chapter 11

Registers and Counters Chapter 12

 Sequential Circuit Analysis & Design

Clocked Sequential Circuit Analysis Chapter 13

Determining State Graphs and Tables Chapter 14

State Table Reduction & State Assignment Chapter 15

Algorithmic State Machine Design Chapter 19

Sequential Circuit Design Chapter 16

 **Special Topics:** (10%)

Arithmetic Circuits (Adders, Multipliers, Dividers) Chapter 18

VHDL, combinational & sequential Chapter 10, 17

**EECE 2030 – Digital Electronics**

**Fall 2010**

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| --- | --- | --- |
| **Section** | 101, MWF 2:00 – 3:15 p |  |
| **Room:** | EN 128 |
| **Instructor:** | Dr. Susan C. SchneiderOffice: HH 217 Phone: 288-7178Mailbox: 51 e-mail: Susan.Schneider@marquette.edu |
| **Office Hours:** | Office hours for instructor posted on office door, listed in D2L course siteOther hours available by appointment |
| **Course Web Site** | If you are registered for this class, you should already be enrolled in the EECE 2030 course on D2L. Review the material on this site frequently and check your e-mail DAILY. |
| **EECE 2030 TAs** | An Ji and Xin (Ryan) Wang |
| **EECE TAs with lab approval authority** | Alex Baker, (hopefully others coming soon) |

**Required Course Materials**:

* Charles H. Roth, Jr. and Larry L. Kinney, Fundamentals of Logic Design, 6th ed., Cengage Learning, 2010. Note - you MUST have the 6th edition, the previous edition is NOT acceptable.Make sure the textbook also has the enclosed CD – possession of this CD provides evidence of your license to use the Direct VHDL software.
* Software resources including MultiSim (installed on the computers in the Digital lab and the EECE Open Lab and on the 4th floor) and Direct VHDL (included on the disk enclosed with the text and installed on all computers in the Digital Electronics Laboratory and the EECE Open Lab).
* EECE 2030 Component Kit.
* The protoboard and wiring kit from the EECE sophomore labs. BIEN students should be able to purchase an equivalent BIEN kit that you will use in subsequent BIEN classes (see Dr. Schneider for more information).
* Laboratory Notebook.

**Optional Course Materials:**

* Marc E. Herniter, *Schematic Capture with MultiSim 7*, Pearson-Prentice-Hall, 2005.

**Attendance:**

Attendance is expected for all class sessions. Excessive absences WILL result in lower grades. The maximum number of absences permitted before lowering a final grade is equivalent to 8 classes; each absence beyond this maximum will result in lowering the final grade at the rate of 1 half letter grade per absence.

**Ethics Policy:**

Any student caught cheating in EECE 2030 will receive an F in the course and be reported to the chair of the EECE department and the Associate Dean of the College of Engineering.

Cheating includes (but is not necessarily limited to):

a. Bringing unauthorized materials into the EECE 2030 test area.

b. Talking to or aiding other students while they are taking a test.

c. Removing any test, test solutions, homework solutions, or study guide solutions from the EECE 2030 classroom without prior permission.

d. Copying any test, lab exercise, design project, or simulation exercise from another student or downloading a possible solution from the internet.

**Grading**:

 Grading will be on the basis of 1400 total points, broken down as follows:

|  |  |
| --- | --- |
| In Class Exams (7 @ 100 pts) | 700 |
| Cumulative Final Exam | 200 |
| Daily Quizzes (best 20 out of 29, @ 10 pts) | 200 |
| Hands-on laboratory activities  | 250 |
|  Exercises (2 @ 25 pts) |  |
|  Design Projects (2 @ 100 pts) |  |
| Participation |  50 |
| Extra Credit  |  |
|  Study Guide completion (15 pts max) | Added to final exam score |
|  DLCI – or – Module Development (5 pts max) | Added to quiz total score |

**Lectures and Study Guides** - For each unit that will be covered this semester, a brief introductory lecture on the material will be given. In addition, each chapter (aka unit) in the textbook has a study guide. The master schedule shows dates for the lectures as well as the dates by which specific study guide unit problems are to be completed. Students are always expected to come to class with specific questions related to the materials they are currently studying and especially so on those days on which no lecture is scheduled.

**Quizzes –**

Daily quizzes will be given according to the master schedule. The topics of each quiz will be determined by the study guide materials that are to be completed on the day of the quiz or were completed 1 or 2 class days prior. Each quiz is a short problem similar to the study guide problems and may have multiple parts. Each quiz is worth 10 pts. There will be a total of 28 quizzes during the semester, your final quiz points will be based on your best 20 quizzes.

**Tests –**

There will be seven (7) tests in this class. Each test will focus on the concepts/topics for several chapters. The master schedule shows the test dates. In general, auxiliary materials – such as “cheat sheets” will NOT be allowed for the tests.

Makeup exams will NOT be given. If you are going to be absent from class on a scheduled test day, please speak with the instructor as soon as possible to arrange to take the test prior to the scheduled date.

**Lab Exercises and Design Projects:**

You will need the EECE 2030 component kit (available in the bookstore) and the tools kit (protoboard and wiring kit), and cable kit from the EECE sophomore labs to complete these assignments. All EECE, COEN, and BIOM – Electrical students should already have the tools and cable kits. BIOM – Computing students may be able to purchase equivalent BIEN lab component kits which will be used in subsequent BIEN labs – see Dr. Schneider.

***Note- all lab assignments should be treated as such. Your preparation work and test procedures and results should be documented in a laboratory notebook. Your laboratory notebook will be reviewed as part of the circuit demonstration.*** The laboratory notebook is the instrument through which all laboratory work is documented. The items that are traditionally included in the laboratory notebook are the design work, simulation results, data tables (with expected values filled in), information about the ICs to be used in the circuits, etc. As we (and the industry) shift to electronic documentation methods, many of these items are originally generated electronically and are therefore easily incorporated into an electronic format such as a Word document or a One-Note workbook for use in preparation (simulations), during lab work (data entry) and after the laboratory work (analysis, reporting). Design work, however, is usually still done “by hand” on paper and needs to be archived appropriately. It is recommended that you use the CoE Laboratory Notebook as your “scratch paper” for the design phase. Scans of the relevant pages from your ‘paper’ lab notebook can be e-mailed to yourself using the MFD printers for incorporation into your report. You may also, if you choose, use the laboratory notebook in the traditional manner for the other aspects such as pasting simulation results into the notebook, entering data into tables you entered into the laboratory notebook, etc. Also (highly frowned on!) you could still do your designs on “any ole” scratch paper and then incorporate the scanned pages into your electronic lab notebook.

***You should also evidence good laboratory skills during your demonstration.*** Good laboratory skills include (but are not necessarily limited to) neat circuit wiring, neat circuit diagrams (with IC pins noted on the schematic) and proper test equipment usage!

The following units have associated laboratory assignments. Additional information about each of the exercises/projects including the rubrics used to assess performance for each of the laboratory assignments and grade sheets are available from the EECE 2030 D2L site.

* **Units 4 and 12** have lab exercises for which you will build and test “simple” digital circuits using discrete gates. A short report is also required. ***Use MultiSim to complete any required simulations*** (NOT LogicAid).
* **Units 8 and 16** have design projects. For these design projects, you will be using a PAL device, the GAL16V8. You will need to read supplemental material that will be provided to you in order to successfully complete the designs. To complete units 8 and 16, you will need to complete and demonstrate your working design solution to the lab TA (or instructor) and submit a short design report for grading by the instructor.

**IMPORTANT – only the EECE 2030 instructor, EECE 2030 TAs or other designated teaching assistants are allowed to certify successful laboratory demonstrations.** This means that if you happen to get your circuit working in the open lab and the attendant TA is not authorized to approve your demonstration, you will still need to come to class to demonstrate it to either an EECE 2030 instructor or one of the EECE 2030 TAs.

**Participation -**  Participation in this class is extremely important and can be evidenced in many different ways. Coming to every class meeting, asking questions, answering instructor questions or the questions of fellow students, working collaboratively with other students on problems, are all ways that an engaged student shows that they are fully participating in the class. To assess your participation, you will complete a self-evaluation of your participation using the Participation Rubric form. The instructor will also complete an evaluation of your participation. Participation will be reviewed TWICE during the semester – at midterm and at the end of class.

The completed self-review Participation Rubric forms are to be uploaded to the appropriate D2L dropbox on October 20 (midterm) and December 10 (end of semester).

**Extra Credit –** Homework is neither assigned nor collected in this class. It is expected that all students will complete the assigned Study Guide problems in a timely manner to remain on target for quizzes and tests. To reward those students who do develop and maintain good study habits for this class, extra credit points will be credited for the timely completion of the Study Guide problems. To earn these extra credit points, students must scan their completed unit study guides and upload to the appropriate D2L drop box no later than the date shown for each unit on the master schedule. These study guides will be reviewed by the instructor and/or TAs and those study guides that show an appropriate amount of correct work will be credited with ONE extra credit point for each unit completed up to a maximum of 15 points.

The extra credit points will be added to the student’s final exam score.

**Grade Scale:**

 A 93%

 AB 89%

 B 85%

 BC 80%

 C 75%

 CD 70%

 D 65%

**OTHER EXTRA CREDIT –** Students will be able to earn an additional 5 extra credit points to be added to the total quiz score by a ONE of two possible ways: (1) EECE 2030 Learning Infrastructure Enhancement **or** (2) participating in the Digital Logic Concept Inventory evaluation.

***(1) EECE 2030 Learning Infrastructure Enhancement*** will consist of an independent project by which the student will develop materials for use in this class by future students. Such projects include, for example, (a) making a video to be posted on D2L which shows how to use the PAL programmer, or (b) creating additional units/chapters including selected readings (from other textbooks and/or the internet), with associated study guide materials including problems for either asynchronous logic design or nano-logic circuits. Students who choose to work on this project must commit to this extra credit option no later than November 1, 2010, and all materials for the project must be submitted no later than December 15, 2010. Contact Dr. Schneider if you are interested in this project.

***(2) Digital Logic Concept Inventory Evaluation*** - Marquette University, EECE Department, (us) has been asked to participate in a nation-wide evaluation of a “Digital Logic Concept Inventory” assessment instrument. The DLCI consists of approximately 24 multiple choice questions on topics which have been covered in this class. The DLCI will take approximately 40 minutes to complete. This assessment will be scheduled for the last week of class. More details will be given to you as they become available. You will be required to complete a consent form if you choose to participate in the evaluation. The scores from the evaluation will be used to assess student mastery of Digital Logic concepts to inform future pedagogy and will NOT be used for individual grades.

|  | **EECE 2030** |  | **MASTER SCHEDULE** |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | Fall 2010 | Lectures, Study Guide, Quizzes, Lab Exercises, Design Projects, Tests, D2L db close |
|   |   | date | Lecture on Unit | Study Guide ProblemsUnit:Problems | Quiz | Test | Lab | D2L dbclose |
|  | M | 30-Aug | 1 |  |  |  |  |  |
| 1 | W | 1-Sep | 2 | 1: all  | 1 |  |  |  |
|   | F | 3-Sep | 3 | 2:1-8 | 2 |   |   | 1 |
|   | M | 6-Sep |   | Labor Day - no class (STUDY)! |   |   |   |
| 2 | W | 8-Sep |  | 2: 9-16, 3:1-4 | 3 |  |  |  |
|   | F | 10-Sep | 4 | 3:5-7 | 4 |   |   | 2 |
|   | M | 13-Sep |   | TEST 1 |   | 1,2,3 |   | 3 |
| 3 | W | 15-Sep | 5 | 4:1-11 | 5 |  | start 4 |  |
|   | F | 17-Sep |   | 5:1-5 | 6 |   |   | 4 |
|  | M | 20-Sep | 6 | 5:6-10 | 7 |  |  |  |
| 4 | W | 22-Sep |   | TEST 2 |   | 4,5 | 4 due | 5 |
|   | F | 24-Sep | 7 | 6:1-4,9 | 8 |   |   |   |
|  | M | 27-Sep |  | 7:1-5 | 9 |  |  | 6 |
| 5 | W | 29-Sep | 9 | 7:5-7 | 10 |  | start 8 |  |
|   | F | 1-Oct | 8 | 9:1-5 | 11 |   |   | 7 |
|  | M | 4-Oct |  | 9:6-8 | 12 |  |  |  |
| 6 | W | 6-Oct |   | TEST 3 |   | 6,7,9 |   | 9 |
|   | F | 8-Oct | 11 | 11:1, 2b-f |   |   | 8 due |   |
|  | M | 11-Oct |  | 11:3b-d,4b-f,5 | 13 |  |  |  |
| 7 | W | 13-Oct | 12 | 11:(4,5),6b-c,7b,8,9 | 14 |  | start 12 |  |
|   | F | 15-Oct |   | 12:1-3 | 15 |   |   | 11 |
|  | M | 18-Oct | 13 | 12:4-5, 13-1 | 16 |  |  |  |
| 8 | W | 20-Oct |   | TEST 4 |   | 11,12 | 12 due | 12 |
|   | F | 22-Oct | Mid Semester Break (STUDY anyway!) |   |
|  | M | 25-Oct |  | 13:2-5 | 17 |  |  |  |
| 9 | W | 27-Oct | 14 | 13:6-7 | 18 |  |  |  |
|   | F | 29-Oct |   | 14:1-4 | 19 |   |   | 13 |
|  | M | 1-Nov |  | 14:5,6,9 | 20 |  |  |  |
| 10 | W | 3-Nov |   | TEST 5 |   | 13,14 |   | 14 |
|   | F | 5-Nov | 15 | 15:1 |   |   |   |   |
|  | M | 8-Nov |  | 15:2-6 | 21 |  |  |  |
| 11 | W | 10-Nov | 16 | 15:7-9 | 22 |  | start 16 |  |
|   | F | 12-Nov | 19 | 15:10-11 | 23 |   |   |   |
|  | M | 15-Nov |  | 19:all | 24 |  |  | 15 |
| 12 | W | 17-Nov |   |  TEST 6 |   | 15,19 |   | 19 |
|   | F | 19-Nov | 18 | 18:1 |   |   |   |   |
|  | M | 22-Nov |  | 18:2 | 25 |  | 16 due |  |
| 13 | W | 24-Nov | Thanksgiving Holiday (you'd better STUDY) |   |
|   | F | 26-Nov |   |
|  | M | 29-Nov |  | 18:3 | 26 |  |  |  |
| 14 | W | 1-Dec |   |  TEST 7 |   | 18 |   | 18 |
|   | F | 3-Dec | 10 |   |   |   |   |   |
|  | M | 6-Dec | 17 | 10:all | 27 |  |  |  |
| 15 | W | 8-Dec |  | 17:all | 28 |  |  |  |
|   | F | 10-Dec |   |   |   |   |   |   |
|  | M | 15-Dec |  |  |  |  |  |  |
|  | T | 14-Dec |  |  |  |  |  |  |
|  | W | 15-Dec |  |  |  |  |  |  |
| FINAL | Th | 16-Dec | 8-10 am | Units 1 - 15 |   |   |   |   |
|  | F | 17-Dec |  |  |  |  |  |  |