Sequential Circuits

Designing with Flip-flops and Registers.

Topics

- Flip-Flops
  - D-FF
  - JK-FF
- Shift Registers
- Design of Sequential Circuits
- Unused states
- Self Correcting Circuits

Flip-Flops

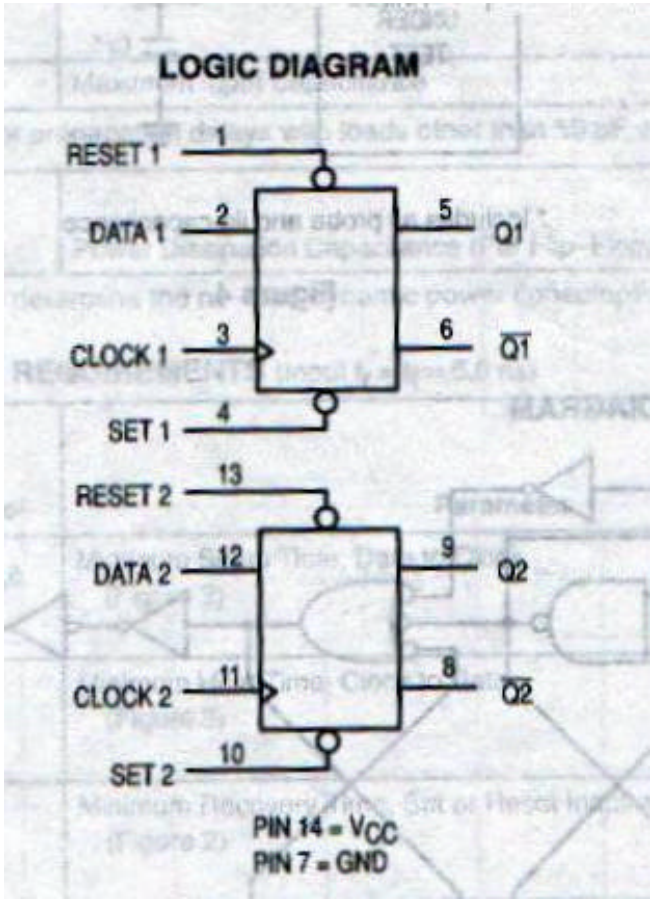
Memory elements used in clocked sequential circuits

Has 2 outputs: one for normal value and one for complement

Maintain a binary state indefinitely until directed to switch states

D Flip-Flops

Ex. 74HC74A Dual D FF w/ Set and Reset



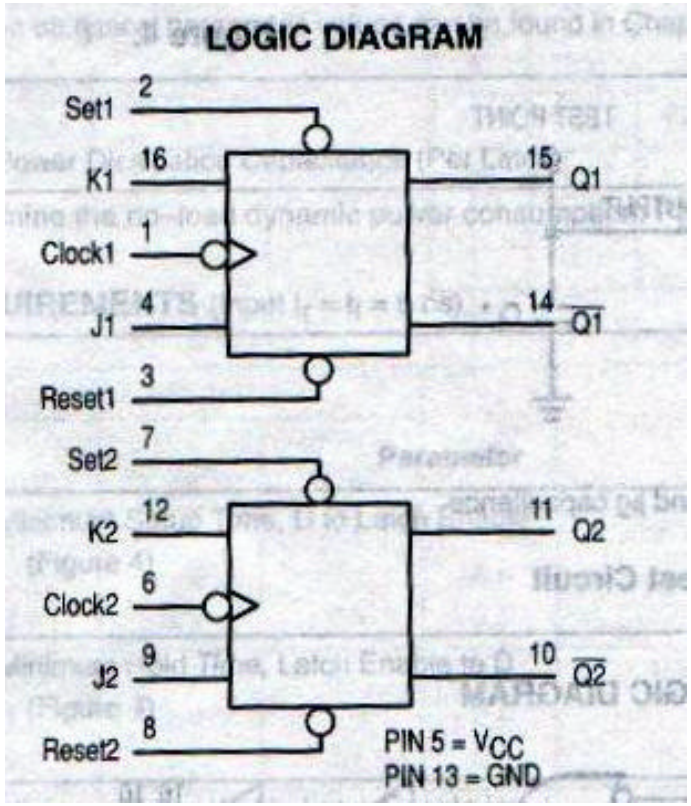
FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

JK Flip-Flops

Ex. 74HC76 Dual JK FF with Set and Reset



FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	No Change	
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	No Change	
H	H	H	X	X	No Change	
H	H	↑	X	X	No Change	

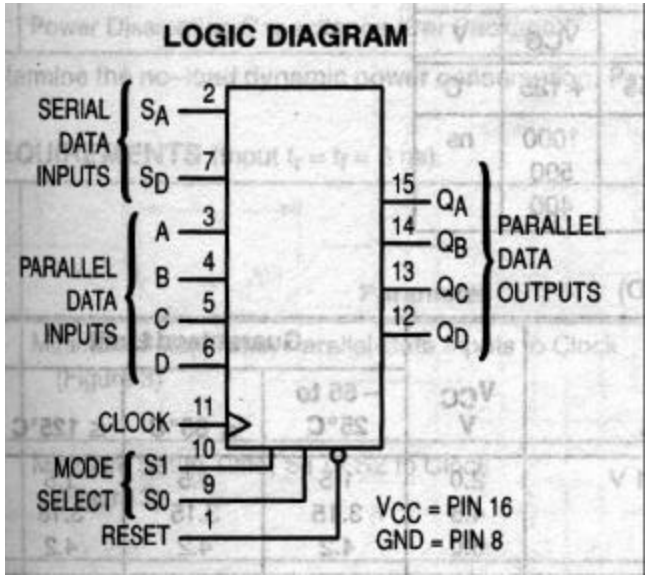
* Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

Registers

- A group of binary storage cells for holding binary information
- Ex. A group of flip-flops
- An N-bit register has N flip-flops
- In addition to FF's a register may have combinational logic to perform data processing tasks.
- LATCH: FF's sensitive to pulse duration
- REGISTER: FF's sensitive to pulse transition

Shift Register

74HC194 4Bit Bidirectional Shift Register



FUNCTION TABLE

Inputs										Outputs				Operating Mode
	Mode Select			Serial Data		Parallel Data								
Reset	S1	S0	Clock	S_D	S_A	A	B	C	D	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	X	X	X	X	X	L	L	L	L	Reset
H	H	H	↑	X	X	a	b	c	d	a	b	c	d	Parallel Load
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Shift Right
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Shift Left
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	
H	L	L	X	X	X	X	X	X	X	No Change				Hold
H	X	X	L	X	X	X	X	X	X	No Change				
H	X	X	H	X	X	X	X	X	X	No Change				

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↑ transition of the clock.

Design of Sequential Circuits

1. Start design with state diagram
2. Complete state table
3. Develop expressions for FF inputs/outputs
4. Create schematic diagrams using appropriate devices

Unused States

- Unused states should be accounted for during the design stages
- Self-Correcting Circuits: Design is able to get out of unused states to some known state

  In design, force unused states to go to known states, with desired outputs

Types of Circuits

- Sequence Recognizer: Sequential circuit that outputs a known signal only after a particular sequence of inputs are applied to the circuit
- Sequence Generator: Sequential circuit that outputs a pre-determined sequence (may or may not depend on the selected input)

Experiment #4: Flip-Flops, Registers & Shift Registers

Goals:

Learn about preset and clear inputs on sequential circuits and their use in state analysis.

Gain experience design, assembly & test of sequential circuits.

Prelab:

1. **Design the sequential circuit for the given state diagram of Figure 4.1.** Use 74HC74 or 74HC76 ICs for Flip-Flops.

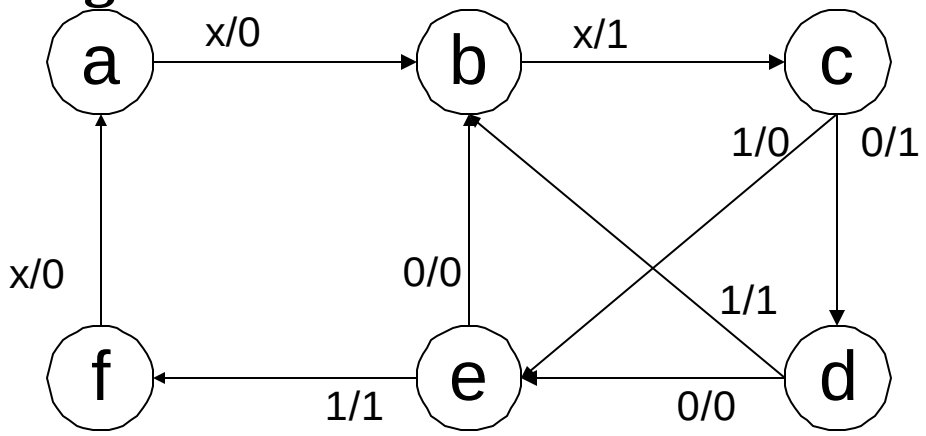


Figure 4.1

2. **Design an 8-bit bi-directional serial shift register.** Include hardware to prevent the shift register from being re-triggered less than 2 seconds after the last trigger.

   An 8-bit word will be parallel loaded when a load switch is enabled.

   Include a serial data input so that the data will then be shifted in the left or right directions based on a direction select input.

8 Bit word is loaded in parallel

Input	Output
01001001	01001001

1 Bit data is shifted in serially in left direction

1	10010011
0	00100110
0	01001100

1 Bit data is shifted in serially in right direction

1	10100110
1	11010011
0	01101001

Experiment Procedure:

Build and test each designed circuit.

Unused State Analysis: Force the sequential cicuit of Figure 4.1 in each unused state and track transitions for each input combination.